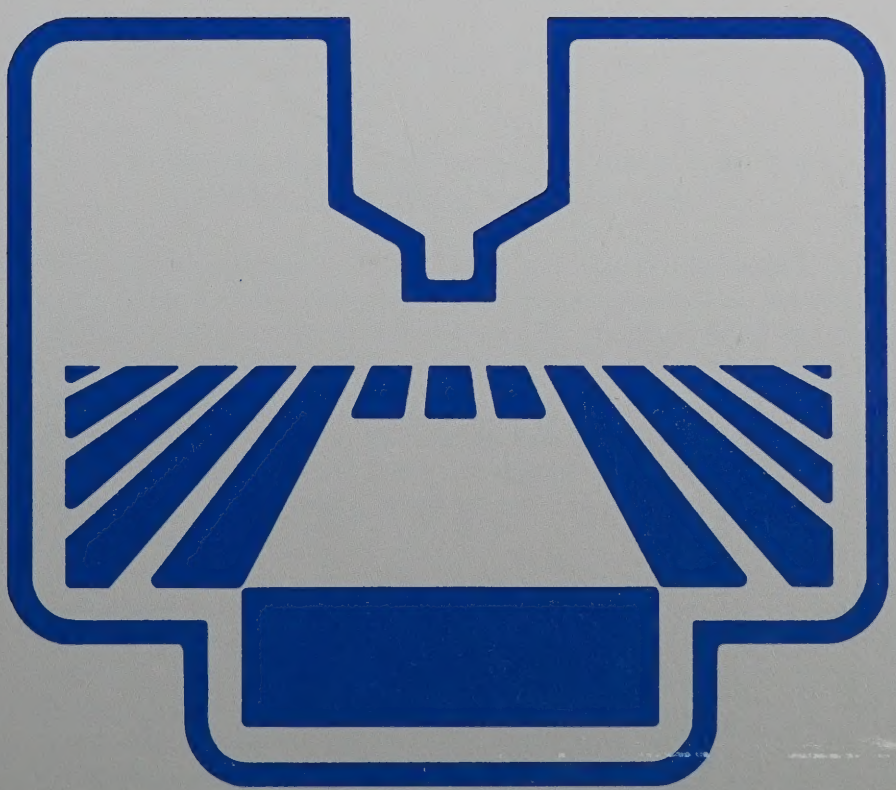
PHILIPS

SMD Process Applications



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SMD Process Applications

Your decision to adopt SMD Technology will result in many opportunities to increase your profits and reduce your manufacturing costs while producing a much more efficient and reliable product.

The Philips family of companies has broad experience in SMD technology:

- Philips companies make the world's broadest line of SMD's. In addition to discrete transistors and diodes in SOT-23, SOT-143, SOT-89, SOD-80, and SOD-87, you can get resistors, capacitors, and IC's in SO and PLCC format in surface mount packages.
- Philips offers an excellent line of automatic pick and place equipment.
- Philips manufactures with SMD technology, making numerous assemblies and subassemblies.

Having pioneered both the SMD packages and the processes to manufacture with them, Philips/Amperex has a unique awareness of the potential problems and suggested solutions found in adopting SMD technology.

The knowledge gained through Philips and Amperex resources is being made available through a series of technical papers, some of which were originally printed by N.V. Philips. The papers are edited by Mark Kastner, Amperex SMD Marketing Manager, for use in the U.S. They cover the following topics:

Substrate Design Guide 3
Thermal Considerations 17
Adhesive Application & Curing 37
Soldering Techniques 47
Solder Joint Criteria 55
Component and Substrate Solderability 63
Fluxing and Cleaning 69
Test and Repair 75
Packaging 79

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Substrate Design Guidelines

An Introduction

SMD Technology embodies a totally new automated circuit assembly process, using a new generation of electronic components: surface mounted devices (SMDs). Smaller than conventional components, SMDs are placed onto the surface of the substrate, not through it like leaded components. And from this, the fundamental difference between SMD assembly and conventional through-hole component assembly arises; SMD component positioning is relative, not absolute.

When a through-hole (leaded) component is inserted into a PCB, either the leads go through the holes, or they don't. An SMD, however, is placed onto the substrate surface, its position only relative to the solder lands, and placement accuracy is therefore influenced by variations in the substrate track pattern, component size, and placement machine accuracy.

Other factors influence the layout of SMD substrates. For example, will the board be a mixed-print (a combination of through-hole components and SMDs) or an all-SMD design? Will SMDs be on one side of the substrate or both? And there are process considerations like what type of machine will place the components and how will they be soldered?

Using our expertise in the world of SMD Technology, this publication, and the others in the series, draw upon applied research in the area of substrate design and manufacture, and present the basic guidelines to assist the designer to make the transition from conventional through-hole PCB assembly to SMD substrate manufacture.

Designing With SMD

SMD Technology is penetrating rapidly into all areas of modern electronic equipment manufacture; in professional, industrial, and consumer applications. Boards are made with conventional print-and-etch PCBs, multilayer boards with thick film ceramic substrates, and with a host of new materials specially developed for SMD assembly.

However, before substrate layout can be attempted, footprints for all components must be defined. Such a footprint will include the combination of patterns for the copper solder lands, the solder resist, and possibly, the solder paste. So the design of a substrate breaks down into two distinct areas: the SMD footprint definition, and the layout and track routing for SMDs on the substrate.

Each of these areas are treated individually in this publication, but first, the general aspects of SMD Technology, including substrate configurations, placement machines, and soldering techniques, are discussed.

Substrate Configurations

SMD substrate assembly configurations are classified as:

Type I—Total surface mount (all-SMD); substrates with no through-hole components at all. SMDs of all types (SM integrated circuits, discrete semiconductors and passive devices) can be mounted either on one side, or both sides of the substrate. See Fig. 1(a).

Type IIA—Double-sided mixed-print; substrates with both through-hole components and SMDs of all types on the top, and smaller SMDs (transistors and passives) on the bottom. See Fig. 1(b).

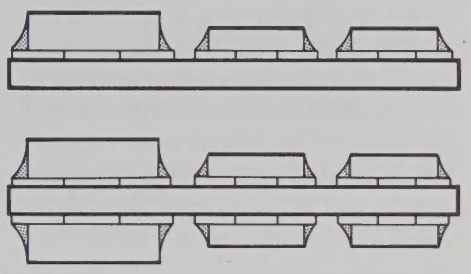


Fig. 1(a) Type I—total surface mount (all-SMD) substrates.

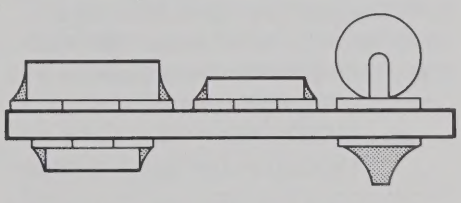


Fig. 1(b) Type IIA—mixed print (double-sided) substrate.

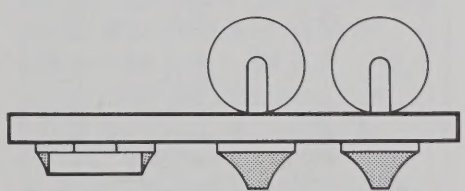


Fig. 1(c) Type IIB—mixed print (underside attachment) substrate.

Type IIB—Underside attachment mixed-print; the top of the substrate is dedicated exclusively to through-hole components, with smaller SMDs (transistor and passives) on the bottom. See Fig. 1(c).

Although the all-SMD substrate will ultimately be the cheapest and smallest variation as there are no through-hole components, it's the mixed-print substrate that many manufacturers will be looking to in the immediate

future, for this technique enjoys most of the advantages of SMD assembly, and overcomes the problem of non-availability of some components in surface mounted form.

The underside attachment variation of the mixed-print (type IIB—which can be thought of as a conventional through-hole assembly with SMDs on the solder side) has the added advantages of only requiring a single-sided print-and-etch PCB, and using the established wave soldering technique. The all-SMD and mixed-print assembly with SMDs on both sides require reflow or combination wave/reflow soldering, and in most cases, a double-sided or multilayer substrate.

The relatively small size of most SMD assemblies compared with equivalent through-hole designs means that circuits can often be repeated several times on a single substrate. This multiple-circuit substrate technique (shown in Fig. 2) further increases production efficiency.

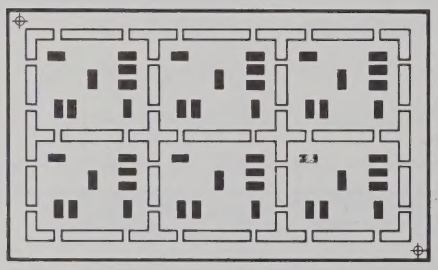


Fig. 2. Multiple-circuit substrate.

Mixed Prints

The possibility of using a partitioned design should be investigated when considering the mixed-print substrate option. For this, part of the circuit would be an all-SMD substrate, and the remainder a conventional through-hole PCB or mixed-print substrate. This allows the circuit to be broken down into, for example, high and low power sections, or high and low frequency sections.

Automated SMD Placement Machines

The selection of automated SMD placement machines for manufacturing requirements is an issue reaching far beyond the scope of this publication. However, as a guide, the four main placement techniques are outlined. They are:

In-line placement—a system with a series of dedicated pick-and-place units, each placing a single SMD in a pre-set position on the substrate. Generally used for small circuits with few components. See Fig 3(a).

Sequential placement—a single pick-and-place unit sequentially places SMDs onto the substrate. The substrate is positioned below the pick-and-place unit using a computer controlled X-Y moving table (a "software programmable" machine). See Fig. 3(b).

Simultaneous placement—places all SMDs in a single operation. A placement module (or station), with a number of pick-and-place units, takes an array of SMDs from the packaging medium and simultaneously places them on the substrate. The pick-and-place units are guided to their substrate location by a program plate (a "hardware programmable" machine), or by software controlled X-Y movement of substrate and/or pick-and-place units. See Fig. 3(c).

Sequential/simultaneous placement—a complete array of SMDs is transferred in a single operation, but the pick-and-place units within each placement module can place all devices simultaneously, or individually (sequentially). Positioning of the SMDs is software controlled by moving the substrate on an X-Y moving table, by X-Y movement of the pick-and-place units, or by a combination of both. See Fig. 3(d).

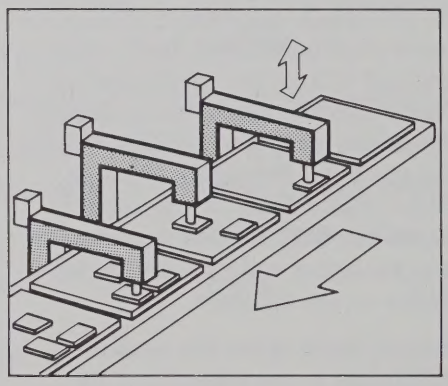


Fig. 3(a) In-line placement.

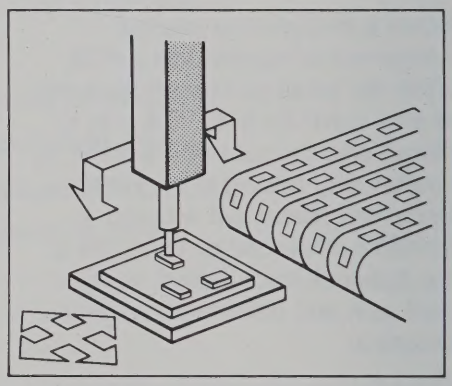


Fig. 3(b) Sequential placement.

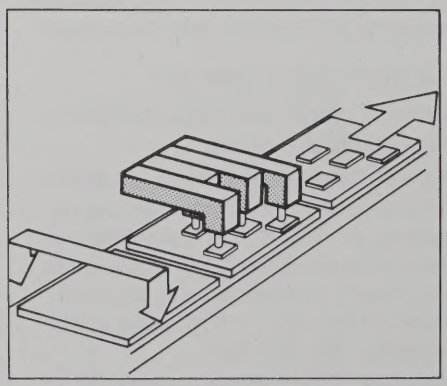


Fig. 3(c) Simultaneous placement.

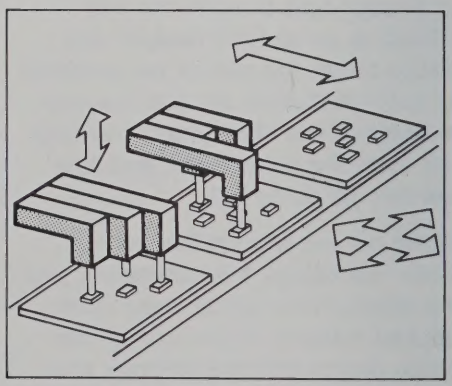


Fig. 3(d) Sequential/simultaneous placement.

All four techniques, although differing in detail, use the same two basic steps; picking the SMD from the packaging medium (tape, magazine or hopper), and placing it on the substrate. In all cases, the exact location of each SMD must be programmed into the automated placement machine.

Soldering Techniques

The SMD populated substrate is soldered by conventional wave soldering, reflow soldering, or a combination of both wave and reflow soldering. These techniques are covered at length in another publication in this series, titled SMD SOLDERING TECHNIQUES, but briefly, they can be described as follows:

Wave soldering—the conventional method of soldering through-hole component assemblies where the substrate passes over a wave (or more often, two waves) of molten solder. This technique is favored for mixed print assemblies with through-hole components on the top of the substrate, and SMDs on the bottom.

Reflow soldering—a technique originally developed for thick-film hybrid circuits using a solder paste or cream (a suspension of fine solder particles in a sticky resin-flux base) applied to the substrate which, after component placement, is heated causing the solder to melt and coalesce. This method is predominantly used for Type I (all-SMD) assemblies.

Combination wave/reflow soldering—a sequential process using both the foregoing techniques to overcome the problems of soldering a double-sided mixed-print substrate, with SMDs and through-hole components on the top, and SMDs only on the bottom. (Type IIB).

Footprint Definition

An SMD footprint, as shown in Fig. 4, consists of:

- a pattern for the (copper) solder lands,
- a pattern for the solder resist,
- if applicable, a pattern for the solder cream.

The design for the footprint can be represented as a set of nominal coordinates and dimensions. In practice,

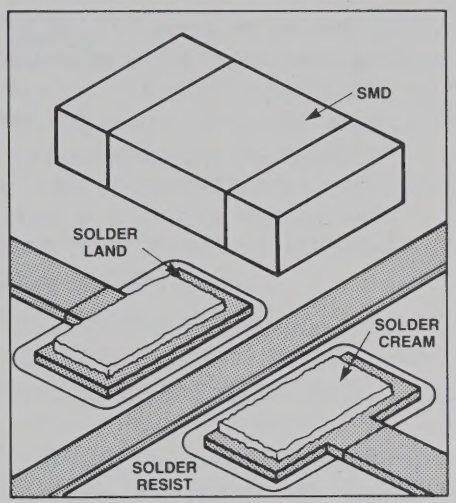


Fig. 4 Component lead, solder land, solder resist and solder cream "footprint."

the actual coordinates of each pattern will be distributed around these nominal values due to positioning and processing tolerances. Therefore the coordinates are stochastic; the actual values form a probability distribution, with a mean value (the nominal value) and a standard deviation.

The coordinates of the SMD are also stochastic. This is due to the tolerances of the actual component dimensions, and the positional errors of the automated placement machine.

The relative positions of solder land, solder resist pattern, and SMD are not arbitrary. A number of requirements may be formulated concerning clearances and overlaps. These include:

- limiting factors in the production of the patterns (for example, the spacing between solder lands or tracks has a minimum value);
- requirements concerning the soldering process (for example, the solder lands must be free of solder resist); and
- requirements concerning the quality of the solder joint (for example, the solder land must protrude from the SMD metallization to allow an appropriate solder meniscus).

Mathematical elaboration of these requirements, and substitution of values for all tolerances and other parameters leads to a set of inequalities that have to be solved simultaneously. To do this manually using worst case design is not considered realistic. A better approach is to use a statistical analysis, and although this requires a complex computer program, it can be done.

Such an approach may deliver more than one solution, and if this is so, then the optimal solution must be determined. Optimization is achieved by setting the following objective: find the solution that:

- minimizes the area occupied by the footprint, and
- maximizes the number of tracks between adjacent solder lands.

The final SMD footprint design also depends on the soldering process to be used. The requirements for a wave soldered substrate differ from those for a reflow soldered substrate, so each is discussed individually.

Footprints For Wave Soldering

To determine the footprint of an SMD for a wave soldered substrate, there are four main interactive factors to consider:

- the component dimensions plus tolerances—determined by the component manufacturer;
- the substrate metallization—positional tolerance of the solder land with respect to a reference point on the substrate;
- the solder resist—positional tolerance of the solder resist pattern with respect to the same reference point; and
- the placement tolerance—the ability of an automated placement machine to accurately position the SMD on the substrate.

The coordinates of patterns and SMDs have to meet a number of requirements. Some of these have a general validity, for example, the minimum overlap of SMD metallization and solderland, and available space

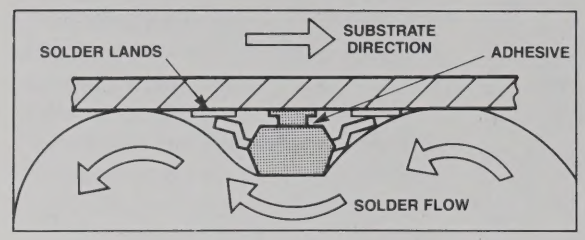


Fig. 5(a) Surface tension can prevent the molten solder reaching the downstream end of the SMD, known as the "shadow effect."

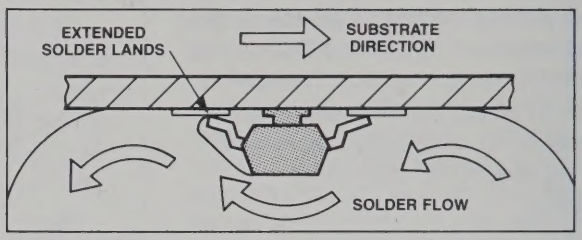


Fig. 5(b) Extending the solder lands to overcome the shadow effect.

for solder maniscus. Others are specifically required to allow successful wave soldering. One has, for example, to take account of factors like the "shadow effect" (missing of joints due to high component bodies), the risk of solder bridging, and the available space for a dot of adhesive.

The "Shadow Effect"

In wave soldering, the way in which the substrate addresses the wave is important. Unlike wave soldering of conventional printed boards, where there are no component bodies to restrict the wave's freedom to traverse across the whole surface, wave soldering of SMD substrates is inhibited by the presence of SMDs on the solder-side of the board. The solder is forced around and over the SMDs as shown in Fig. 5(a), and the surface tension of the molten solder prevents it reaching the far end of the component, resulting in a dry-joint downstream of the solder flow. This is known as the "shadow effect."

The shadow effect becomes critical with high component bodies. However, wetting of the solder lands during wave soldering can be improved by enlarging each land as shown in Fig. 5(b). The extended substrate metallization makes contact with the solder, allowing it to flow back and around the component metallization to form the joint.

The use of the dual-wave soldering technique also partially alleviates this problem because the first, turbulent wave has sufficient upward pressure to force solder onto the component metallization, and the second, smooth wave "washes" the substrate to form good fillets of solder. Similarly, oil on the surface of the solder wave lowers the surface tension, which lessens the shadow effect, but this technique introduces problems of contaminants in the solder when the oil decomposes.

Footprint Orientation

The orientation of SO (small outline) and VSO (very small outline) ICs is critical on wave-soldered substrates for the prevention of solder bridge formation. Optimum solder penetration is achieved when the central axis of the IC is parallel to the flow of solder as shown in Fig. 6(a). The SO package may also be transversly oriented, as shown in Fig. 6(b); but, this is totally unacceptable for the VSO package.

Solder Thieves

Even with parallel mounted SO and VSO packages, solder-bridges have a tendancy to form on the leads downstream of the solder flow. The use of solder thieves (small squares of substrate metallization), shown in Fig. 7 for a 40-pin VSO, further reduces the likelihood of solder-bridge formation.

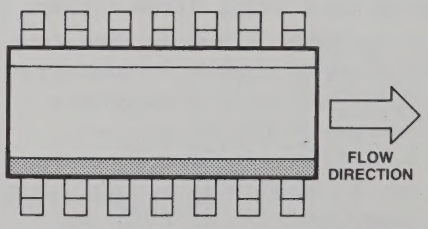


Fig. 6(a) Parallel orientation for SO and VSO packages.

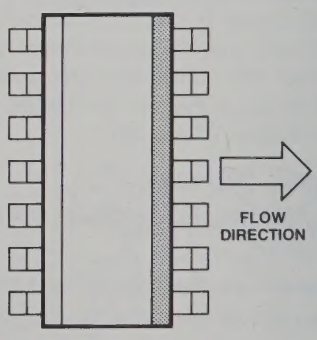


Fig. 6(b) Transverse orientation for SO packages only.

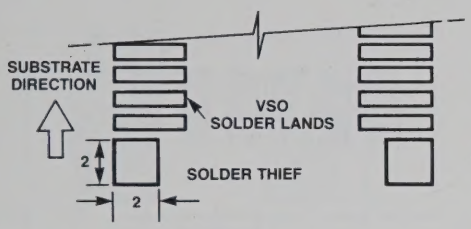


Fig. 7 Example of solder thieves for VSO-40 footprints (dims in mm).

Placement Inaccuracy

Another major cause of solder bridges on SO ICs and plastic leaded chip carriers (PLCCs) is a slight misalignment as shown in Fig. 8. The close spacing of the leads on these devices means that any inaccuracy in placement drastically reduces the space between adjacent pins and solder lands thus increasing the chance of solder bridges forming.

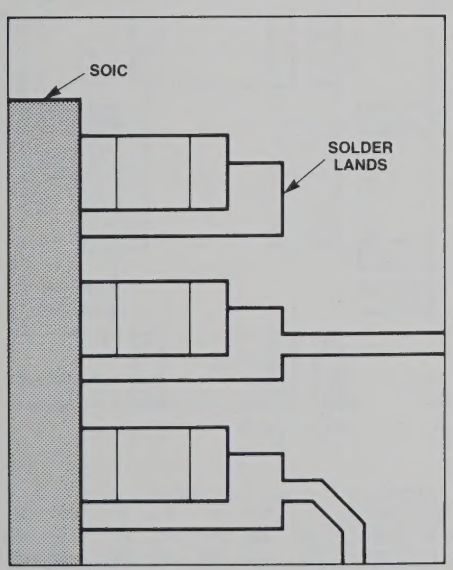


Fig. 8 Misaligned placement of SO package increases the possibility of solder bridging.

Dummy Tracks For Adhesive Application

For wave soldering, an adhesive to affix components to the substrate is required. This is necessary to hold the SMDs in place between the placement operation and the soldering process (this technique is covered at length in another publication in this series, titled ADHESIVE APPLICATION AND CURING).

The amount of adhesive applied is critical for two reasons: first, the adhesive dot must be high enough to reach the SMD, and second, there mustn't be too much adhesive which could foul the solder land and prevent the formation of a solder joint. The three parameters governing the height of the adhesive dot are shown in Fig. 9. Although this diagram illustrates that the minimum requirement is $C > A + B$, in practice, $C > 2(A + B)$ is more realistic for the formation of a good strong bond.

Taking these parameters in turn, the substrate metallization height (A), can range from about 35 μm for a normal print-and-etch PCB, to 135 μm for a plated-through-hole board. And the component metallization height (B), for example on 1206 size passive devices, may differ by several tens of microns. Therefore, A + B can vary considerably, but it is desirable to keep the dot height (C) constant for any one substrate.

The solution to this apparent problem is to route a track under the device, as shown in Fig. 10. This will eliminate the substrate metallization height (A), from the adhesive dot-height criteria. Quite often, the high component density of SMD substrates necessitates the routing of tracks between solder lands, and where it does not, a short dummy track should be introduced.

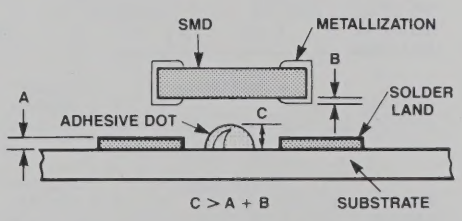
For bonding small outline (SO) ICs to the substrate, two dots of adhesive are sufficient for SO-8, 14 and 16 pin packages, but the SOL-20, 24, 28 and VSO-40 pin packages need three dots. The through-tracks (or dummy tracks) must be positioned beneath the IC accordingly to support the adhesive dots.

Footprints For Reflow Soldering

To determine the footprint of an SMD for a reflow soldered substrate, there are now five interactive factors to consider. The four that effect the wave solder footprints (although the solder resist may be omitted), plus an additional factor relating to the solder cream application. That is, the positional tolerance of the screen printed solder cream with respect to the solder lands.

Solder Cream Application

In reflow soldering, the solder cream (or paste) is applied by pressure syringe dispensing, or by screen printing. For industrial purposes, screen



A = Substrate metallization height
B = SMD metallization height
C = Height of adhesive dot

Fig. 9 Adhesive dot height criteria.

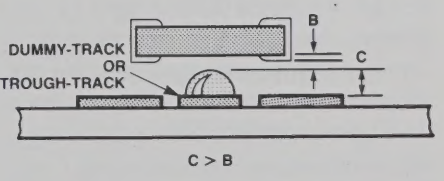


Fig. 10 Through-track or dummy track to modify dot height criteria.

printing is the favored technique, as it is much faster than dispensing.

Screen Printing

A stainless steel mesh, coated with emulsion except for the solder land pattern where cream is required, is placed over the substrate. A squeegee passes across the screen and forces solder cream through the uncoated areas of the mesh and onto the solder land. As a result, dots of solder cream of a given height and density (in mg/mm^2) are produced.

There is an optimum amount of solder cream for each joint. For example, the solder cream requirements for the C1206 SM capacitor is around 1.5 mg per end, and for the SO IC between 0.5 and 0.75 mg per lead is required.

The solder cream density, combined with the required amount of solder, makes a demand upon the area of the solder land (in mm^2). The footprint dimensions for the solder cream pattern are typically identical to those for the solder lands.

Floating

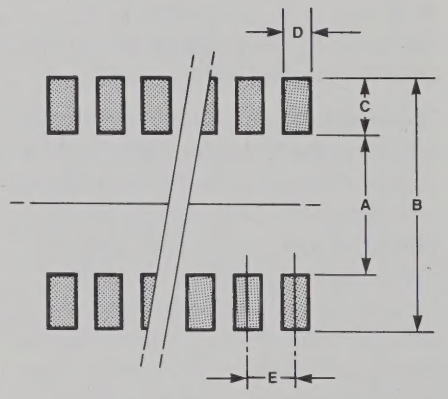
One phenomenon sometimes observed on reflow soldered substrates is that known as "floating" (or "swimming"). This occurs when the solder paste reflows, and the force exerted by the surface tension of the now molten solder "pulls" the SMD to the center of the solder land.

When the solder reflows at both ends simultaneously, the swimming phenomenon results in the SMD self-centering on the footprint as the forces of surface tension fight for equilibrium. Although this effect can remove minor positional errors, it's not a dependable feature and cannot be relied upon. Components must always be positioned as accurately as possible.

Footprint Dimensions

The following diagrams (Fig. 11 to 19) show footprint dimensions for SO ICs, the VSO-40 package, PLCC packages, and the range of surface mounted transistors, diodes, resistors and capacitors. All dimensions given are based on the criteria discussed in these guidelines.

Please note—these footprints are based on our experience with both experimental and actual production substrates, and are reproduced for guidance only. Research is constantly going on to cover all SMDs currently available, and those planned for the future, and data will be published when it becomes available.



INCHES

PACKAGE OUTLINE	A	B	C	D	E
SO-8, 14, 16	.155	.275	.060	.024	.050
SOL-16, 20, 24, 28	.310	.450	.070	.024	.050

METRIC (mm)

PACKAGE OUTLINE	A	B	C	D	E
SO SMALL	4.0	7.0	1.5	.6	1.27
SO LARGE	7.8	11.4	1.8	.6	1.27

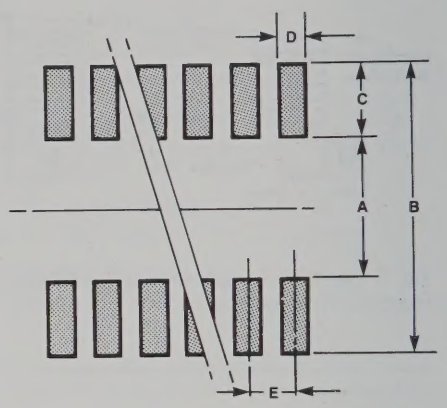
METRIC (mm)

PACKAGE OUTLINE	A	B	C	D	E
SOL-8	9.0	13.2	2.1	.6	1.27

INCHES

PACKAGE OUTLINE	A	B	C	D	E
SOL-8	.36	.528	.084	.024	.050

Fig. 11 Footprints for SO ICs.



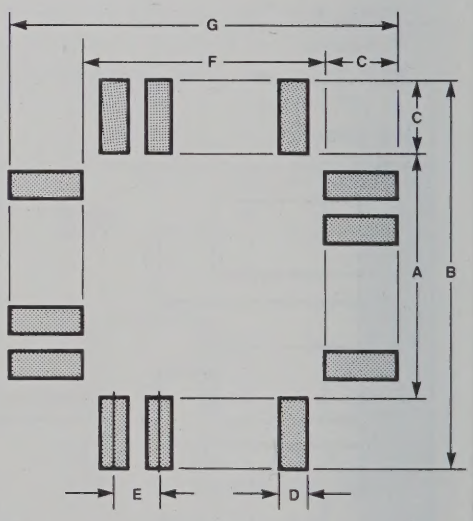
INCHES

PACKAGE OUTLINE	A	B	C	D	E
VSO-40	.32	.536	.108	.02	.030
VSO-56	.46	.676	.108	.02	.030

METRIC (mm)

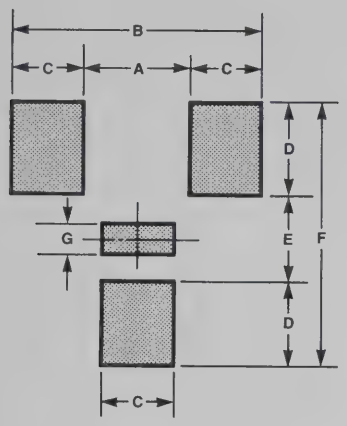
PACKAGE OUTLINE	A	B	C	D	E
VSO-40	8.0	13.4	2.7	.5	.762
VSO-56	11.5	16.9	2.7	.5	.75

Fig. 12 Footprints for VSO ICs.



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G
PLCC-20	.260	.440	.090	.024	.050	.260	.440
PLCC-28	.360	.540	.090	.024	.050	.360	.540
PLCC-44	.560	.740	.090	.024	.050	.560	.740
PLCC-52	.660	.840	.090	.024	.050	.660	.840
PLCC-68	.860	1.040	.090	.024	.050	.860	1.040
PLCC-84	1.060	1.240	.090	.024	.050	1.060	1.240
PLCC-32	.360	.540	.090	.024	.050	.460	.640

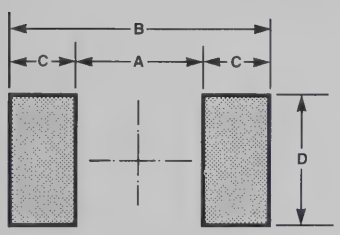
Fig. 13 Footprints for PLCCs.



SOT-23	INCHES A	B	C	D	E	F
Reflow	.048	.104	.028	.044	.104	—
Wave	.032	.136	.052	.052	.048	.152

SOT-23	METRIC (mm) A	B	C	D	E	F
Reflow	1.2	2.6	.7	1.1	2.6	—
Wave	.8	3.4	1.3	1.3	1.2	3.8

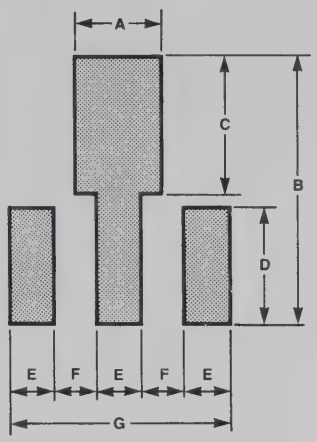
Fig. 14 Footprints for SOT-23 transistors.



SOD-80	INCHES A	B	C	D
Reflow	.096	.208	.056	.056
Wave	.10	.2	.05	.08

SOD-80	METRIC (mm) A	B	C	D
Reflow	2.4	5.2	1.4	1.4
Wave	2.5	5.0	1.25	2.0

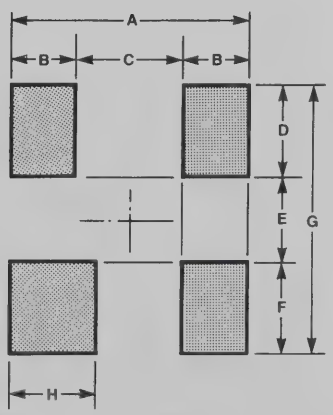
Fig. 15 Footprints for SOD-80 diodes.



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G
SOT-89	.08	.184	.104	.048	.032	.028	.152

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E	F	G
SOT-89	2.0	4.6	2.6	1.2	.8	.7	3.8

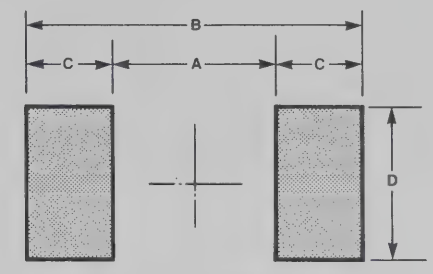
Fig. 16 Footprints for reflow soldered SOT-89 transistors.



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G	H
SOT-143	.104	.028	.048	.036	.044	.036	.116	.044

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E	F	G	H
SOT-143	2.6	.7	1.2	.9	1.1	.9	2.0	1.1

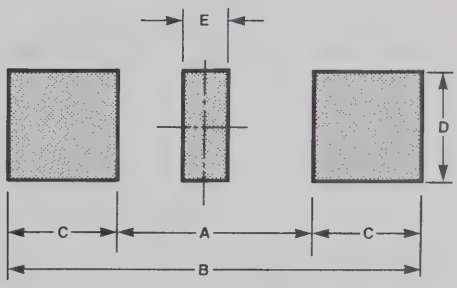
Fig. 17 Footprints for reflow soldered SOT-143 transistors.



CODE	SIZE	INCHES A	B	C	D
C0805	.08 × .05	.032	.136	.052	.056
R/C1206	.128 × .064	.072	.184	.056	.068
C1210	.128 × .1	.072	.184	.056	.104
C1808	.18 × .08	.112	.248	.068	.084
C1812	.18 × .128	.112	.248	.068	.132
C2220	.228 × .2	.16	.296	.068	.204

CODE	SIZE	METRIC A	B	C	D
C0805	2.0 × 1.25	0.8	3.4	1.3	1.4
R/C1206	3.2 × 1.6	1.8	4.6	1.4	1.7
C1210	3.2 × 2.5	1.8	4.6	1.4	2.6
C1808	4.5 × 2.0	2.8	6.2	1.7	2.1
C1812	4.5 × 3.2	2.8	6.2	1.7	3.3
C2220	5.7 × 5.0	4.0	7.4	1.7	5.1

Fig. 18 Footprints for reflow soldered surface mounted resistors and ceramic multilayer capacitors.



	SIZE	INCHES A	B	C	D	E
C0805	.08 × .05	.048	.144	.048	.048	.016
R/C 1206	.128 × .064	.08	.192	.056	.056	.020

CODE	SIZE	METRIC (mm) A	B	C	D	E
C0805	2.0 × 1.25	1.2	3.6	1.2	1.2	0.4
R/C1206	3.2 × 1.6	2.0	4.8	1.4	1.4	0.5

Fig. 19 Footprints for wave soldered surface mounted resistors and ceramic multilayer capacitors.

Layout Considerations

Component orientation plays an important role in obtaining consistent solder-joint quality. The substrate layout shown in Fig. 20 will result in significantly better solder joints than a substrate with SMD resistors and capacitors positioned parallel to the solder flow.

Component Pitch

The minimum component pitch is governed by the maximum width of the component and the minimum distance between adjacent components. When defining the maximum component width, the rotational accuracy of the placement machine must also be considered. Figure 21 shows how the effective width of the SMD is increased when the component is rotated with respect to the footprint by angle ϕ° (for clarity, the rotation is exaggerated in the illustration).

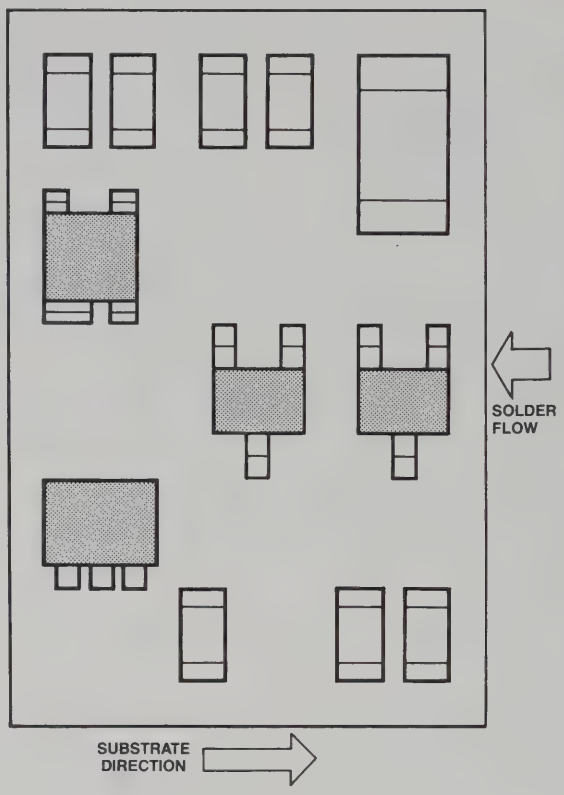
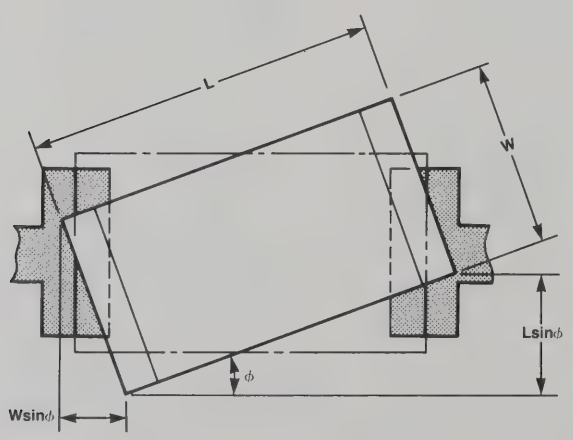


Fig. 20 Recommended component orientation for wave soldered substrates.



ϕ = Component rotation with respect to footprint
L sin ϕ = Effective increase in width
W sin ϕ = Effective increase in length

Fig. 21 The influence of rotation of the SMD with respect to the footprint.

The minimum permissible distance between adjacent SMDs is a figure based upon the gap required to avoid solder-bridging during the wave soldering process. Figure 22 shows how this distance, plus the maximum component width, are combined to derive the basic expression for calculating the minimum pitch (F_{min}).

As a guide, the recommended minimum pitches for various combinations of two sizes of SMDs, the R/C1206 and C0805 (R or C designating resistor or capacitor respectively, the number referring to the component size), are given in *Table 1*. These figures are statistically derived under certain assumed boundary conditions, as follows:

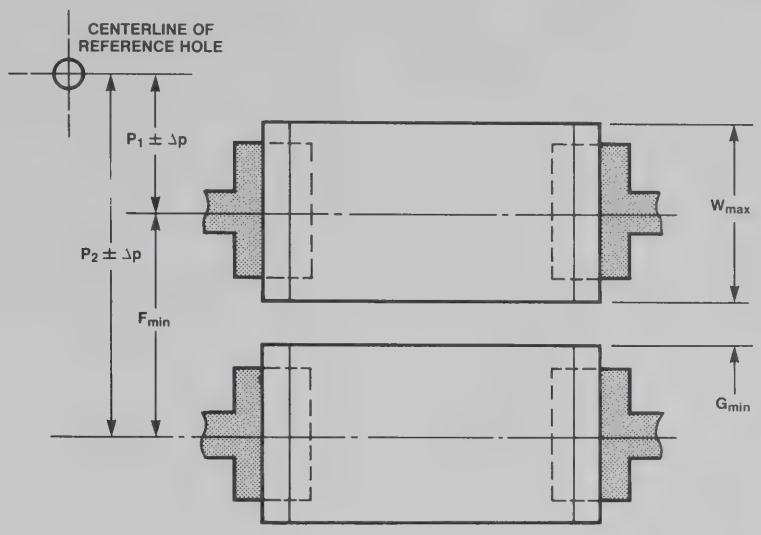
- positioning error (Δp) ±0.3 mm; (± .012″)
- pattern accuracy (Δq) ±0.3 mm; (±.012″)
- rotational accuracy (ϕ) ±3°;
- component metallization/solder land overlap (M_{min}) 0.1 mm (.004″) (note this figure is only valid for wave soldering);
- the figure for the minimum permissible gap between adjacent components (G_{min}) is taken to be 0.5 mm (.020″).

As these calculations are not based on worst-case conditions, but on a statistical analysis of all boundary conditions, there is a certain flexibility in the given data.

For example, it is possible to position R/C1206 SMDs on a 2.5 mm pitch, but the probability of component placements occurring with G_{min} smaller than 0.5 mm will increase, hence the likelihood of solder-bridging also increases. Each application must be assessed on individual merit, with regard to acceptable levels of re-work and so on.

Solder Land/Via Hole Relationship

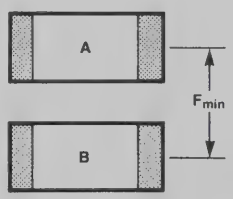
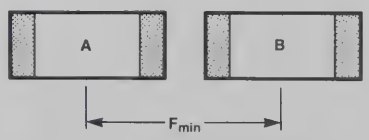
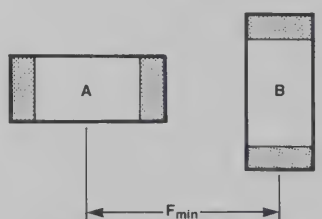
With relow soldered multilayer and double-sided plated-through-hole substrates, there must be sufficient separation between the via holes and the



W_{max} = Maximum width of component
G_{min} = Minimum permissible gap
F_{min} = Minimum pitch
P_1 = Nominal position of component 1 (tolerance Δp)
P_2 = Nominal position of component 2 (tolerance Δp)
F_{min} = $W_{max} + 2\Delta p + G_{min}$

Fig. 22 Criteria for determining the minimum pitch of SMDs.

Table 1 Recommended Pitch For R/C1206 and C0805 SMDs

Combination	Component A	Component B R/C1206	Component B C0805
	R/C1206	3.0 (.12″)	2.8 (.112″)
	C0805	2.8 (.112″)	2.6 (.104″)
	R/C1206	5.8 (.232″)	5.3 (.212″)
	C0805	5.3 (.212″)	4.8 (.192″)
	R/C1206	4.1 (.164″)	3.7 (.148″)
	C0805	3.6 (.144″)	3.0 (.12″)

(inches in parentheses)

solder lands to prevent a solder-well forming. If too close to a solder joint, the via hole may suck the molten solder away from the component by capillaric action, resulting in insufficient wetting of the joint.

Solder Land/Component Lead Relationship

A special consideration for mixed print substrate layout is the location of leaded components with respect to the SMD footprints, and the minimum distance between a protruding clinched lead and a conductor or SMD. Figure 23 shows typical configurations for R/C1206 SMDs mounted on the underside of a substrate with respect to the clinched leads of a leaded component. Minimum distances between the clinched lead ends and the SMDs or substrate conductors are 1 mm (.04″) and 0.5 (.02″) respectively.

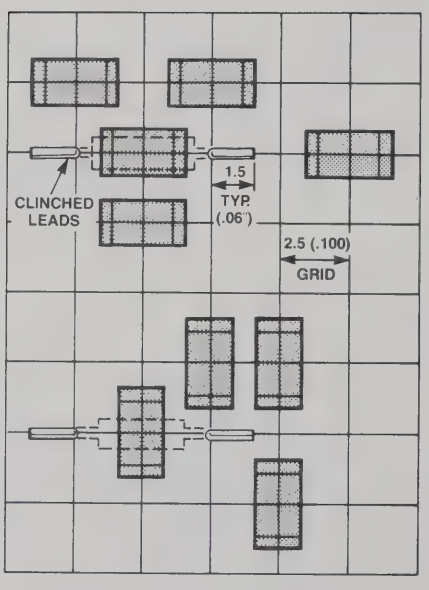


Fig. 23 Location of R/C1206 SMDs on the underside of a mixed print substrate with respect to the clinched leads of through-hole components (dimensions in mm).

Placement Machine Restrictions

There are two ways of looking at the distribution of SMDs on the substrate: uniform SMD placement, and non-uniform SMD placement. With non-uniform placement, center-to-center dimensions of SMDs are not exact multiples of a pre-determined dimension as shown in Fig. 24(a), so the location of each is difficult to program into the machine.

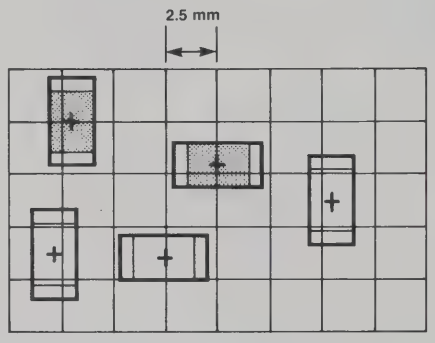


Fig. 24(a) Non-uniform component placement.

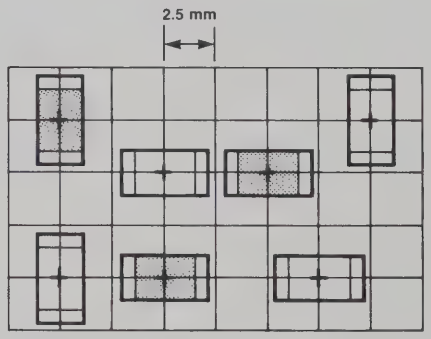


Fig. 24(b) Uniform component placement.

Uniform placement uses a modular grid system with devices placed on a uniform center-to-center spacing, for example, 2.5 (.1″) or 5 mm (.2″) as shown in Fig. 24(b). This has the distinct advantage of establishing a standard, enabling the use of other automated placement machines for future production requirements without having to redesign boards.

Substrate Population

Population density of SMDs over the total area of the substrate must also be carefully considered, as placement machine limitations can create a "lane" or "zone" that restricts the total number of components which can be placed within that area on the substrate.

For example, on a hardware-programmable simultaneous placement machine (see Fig. 3(c)), each pick-and-place unit within the placement module can only place a component on the substrate in a restricted lane (owing to adjacent pick-and-place units), typically 10 to 12 mm (.4″ to .48″) wide, as shown in Fig. 25.

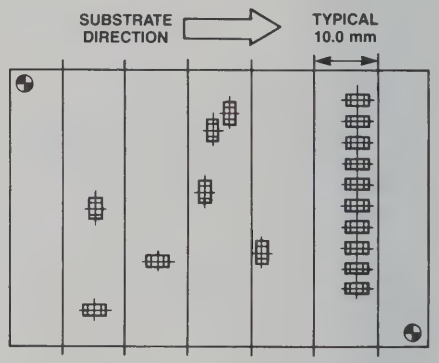


Fig. 25 Substrate "lanes" from use of a simultaneous placement machine.

Placement of the 10 components in the lane on the right of the substrate shown will require a machine with 10 placement modules (or ten passes beneath a single placement module), an inefficient process considering that there are no more than three SMDs in any other lane.

Test Points

Siting of test-points for in-circuit testing of SMD substrates presents problems owing to the fewer via-holes, higher component densities, and components on both sides of SMD substrates. On conventional

double-sided PCBs, the via holes and plated-through component lead-holes means that most test-points are accessible from one side of the board. However, on SMD substrates, extra provision for test-points may have to be made on both sides of the substrate.

Figure 26(a) shows the recommended approach for positioning test-points in tracks close to components, and Fig. 26(b) shows an acceptable, though not recommended alternative, where the solder land is exended to accommodate the test-pin. This latter method avoids sacrificing too much board space thus maintaining a high-density layout, but can introduce the problem of components moving ("floating") when reflow soldered.

The approch shown in Fig. 26(c) is totally unacceptable, as the pressure applied by the test-pin can make an open-circuit soldered joint appear to be good, and more importantly, the test-pin can damage the metallization on the component, particularly with small SMDs.

CAD Systems For SMD Substrate Layout

At present, about half of all PCBs are laid out using computer-aided design (CAD) techniques, and this proportion is expected to rise to over 90 per cent by 1988. Of the many current CAD systems available for designing PCB layouts for conventional through-hole components and ICs in DIL packages, few are SMD-compatible, and systems dedicated exclusively to SMD substrate layout are still comparatively rare. There are two main reasons for this: some CAD suppliers are waiting for SMD technology to fully mature before updating their systems to cater to SMD-loaded substrates, and others are holding back until standard package outlines are fully defined.

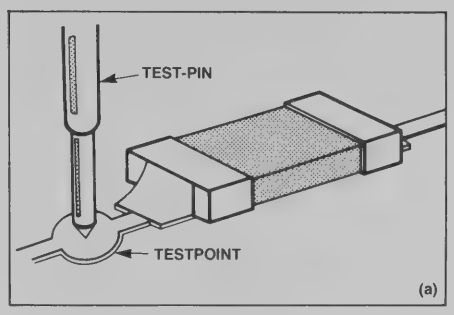


Fig. 26(a) RECOMMENDED test point location close to an SMD.

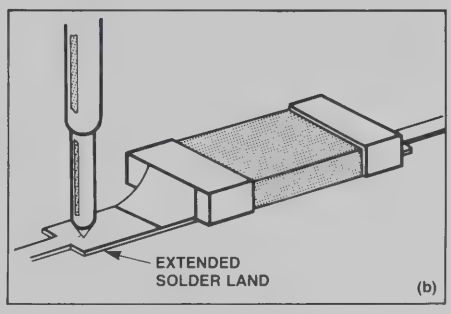


Fig. 26(b) Acceptable test point location.

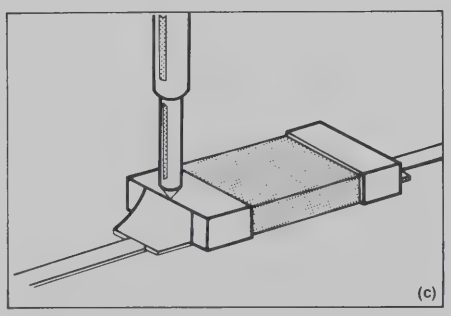


Fig. 26(c) UNACCEPTABLE test point location.

However, updating CAD systems used for through-hole printed boards is not simply a case of substituting SMD footprints for conventional component footprints, since SMD-populated substrates impose far tougher restraints on PCB layout and require a total rethink of the layout programs. For example, systems must deal with higher component densities, finer track widths, devices on both sides of the substrate (possibly occupying corresponding positions on opposite sides), and even SMDs under conventional DILs on the same side of the substrate.

The amount of re-working that a program requires depends on whether it's an interactive (manual) system, or one with fully automatic routing and placement capabilities. For interactive systems, where the user positions the components and routes the tracks manually on-screen, program modifications will be minimal. Automatic systems, however, must contend with the stricter design rules for SMD substrate layout. For example, many autorouting programs assume that every solder land is a plated-through-hole, and therefore can be used as a via-hole. This is not applicable for SMD populated substrates.

CAD programs base the substrate layout on a regular grid. This method, analogous to drawing the layout on graph paper, must have the grid lines on a pitch that is no larger than the smallest component or feature (track width, pitch, and so on). For conventional DIL boards, this is typically 0.635 mm (0.025″), but with the much smaller SMDs, a grid spacing of 0.0254 mm (0.001″) is required. Consequently, for the same area of substrate, a CAD system based on this finer grid requires a resolution more than 600 times greater than that for conventional layout CAD systems.

To handle this, extra memory capacity can be added, or the allowable substrate area can be limited. In fact, the small size of SMDs, and the high-density layouts possible, generally results in a smaller substrate. However, high density layout gives rise to additional complications not directly related to the SMD substrate design guidelines. Most CAD systems, for instance, cannot always completely route all interconnects, and some traces have to be routed manually. This can be particularly difficult with the fewer via-holes and smaller component spacing of SMD boards.

Ideally, the CAD program should have a "tear-up and start again" algorithm that allows it to re-start autorouting if a previous attempt reaches a position where no further traces can be routed before an acceptable percentage of interconnects (and this percentage must first be determined) have been made. This minimizes the manual reworking required.

CAE/CAD/CAM Interaction

Computer-aided production of printed boards has evolved from what was initially only a computer-aided manufacturing process (CAM—digetising a manually generated layout and using a photoplotter to produce the artwork) to fully interactive computer-aided engineering, design and manufacture using a common data base. Figure 27 illustrates how this multi-dimensional interaction is particularly suited to SMD-populated substrate manufacture in its highly automated environment of pick-and-place assembly machines and test equipment.

Using a fully integrated system, linked by local area network to a central data base, will make it possible to use the initial computer-aided engineering (CAE—schematic design, logic verification and fault simulation) in the generation of the final test-patterns at the end of the development process. These test-patterns can then be used with the automatic test equipment (ATE) for functional testing of the finished substrates.

Such a system is particularly useful for testing SMD-populated substrates, as their high component density and fewer via-holes make in-circuit testing ("bed of nails" approach) difficult. Consequently, manufacturers are turning to functional testing as an alternative. (These aspects are covered in another publication in this series titled *Functional Testing And Repair*).

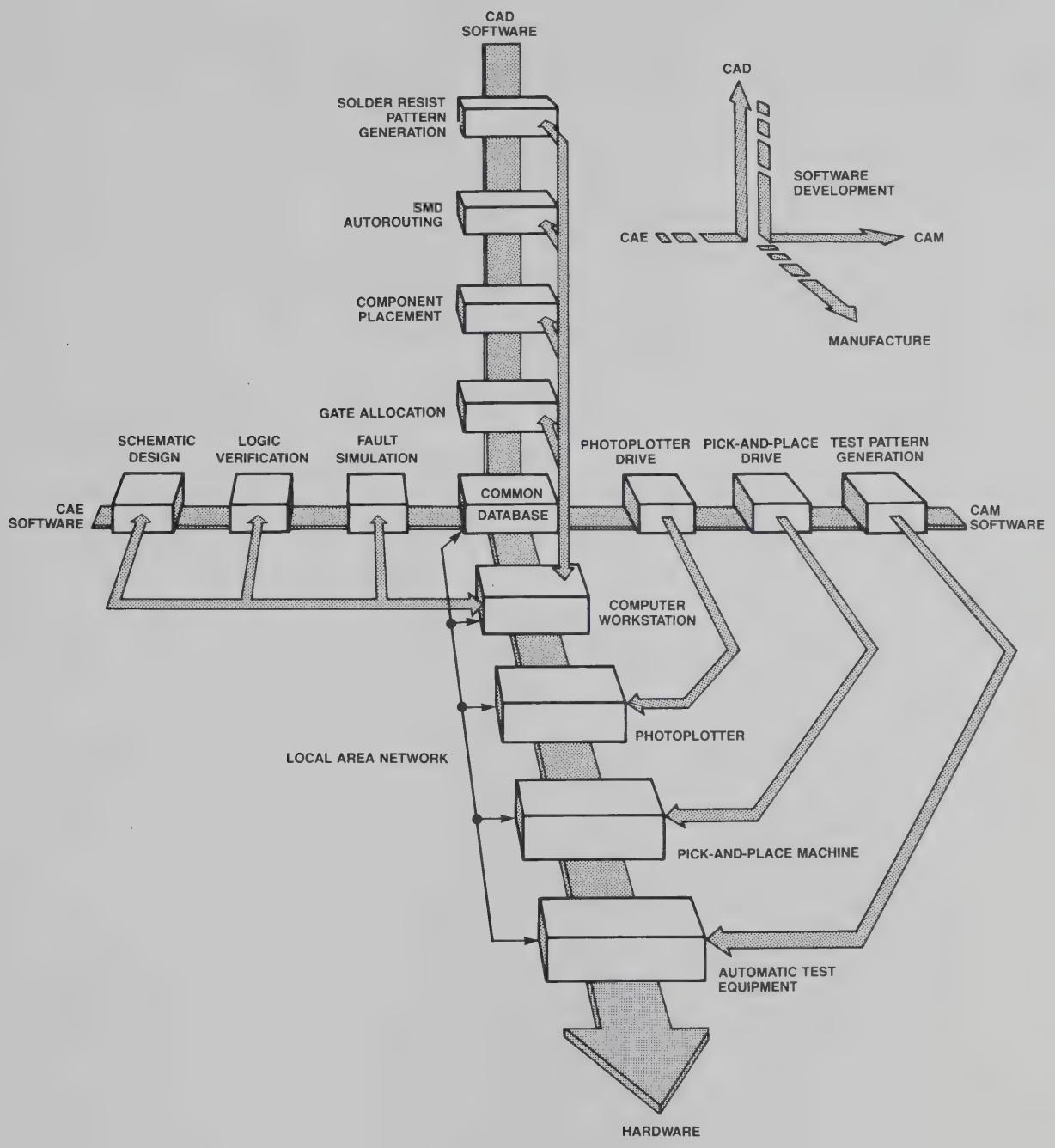


Fig. 27 The software-hardware interaction for the computer-aided engineering, design and manufacture of SMD substrates.

Thermal Considerations

INTRODUCTION

Thermal characteristics of integrated circuit (IC) packages have always been a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can have an adverse effect on the long term operating life of an IC. As will be shown in this paper, the advantages realized by miniaturization can often have trade-offs in terms of increased junction temperatures. Some of the **VARIABLES affecting T_J are controlled by the PRODUCER of the IC, while others are controlled by the USER and the ENVIRONMENT in which the device is used.**

With the increased use of Surface Mount Device (SMD) technology, management of thermal characteristics remains a valid concern because not only are the SMD packages much smaller, but the thermal energy is concentrated more densely on the printed wiring board (PWB). For these reasons, the designer and manufacturer of surface mount assemblies (SMAs) must be more aware of all the variables affecting T_J.

POWER DISSIPATION

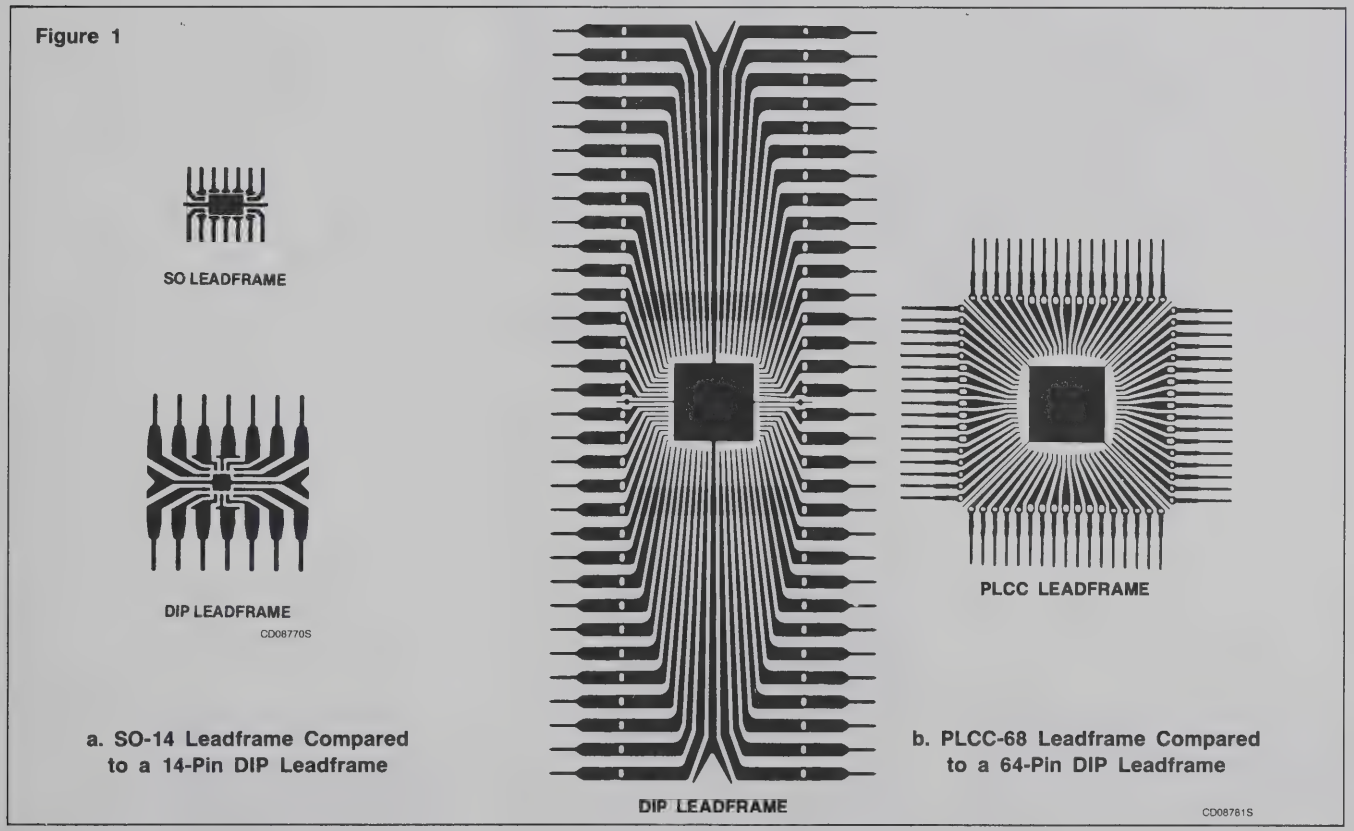
Power dissipation (P_D), varies from one device to another and can be obtained by multiplying V_{CC} Max by typical I_{CC}. Since I_{CC} decreases with an increase in temperature, maximum I_{CC} values are not used.

THERMAL RESISTANCE

The ability of the package to conduct this heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta JA (θ_{JA}). θ_{JA} is often separated into two components: thermal resistance from the junction to case, and the thermal resistance from the case to ambient. θ_{JA} represents the total resistance to heat flow from the chip to ambient and is expressed as follows:

$$\theta_{JC} + \theta_{CA} = \theta_{JA}$$

Figure 1



**Data contained in this paper was developed at N.V. Philips and the Signetics Package Engineering Lab.*

Edited by Mark Kastner and Paul Melville

JUNCTION TEMPERATURE (T_J)

Junction temperature (T_J) is the temperature of a powered IC measured by Signetics at the substrate diode. When the chip is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A). T_J is calculated by multiplying the power dissipation of the device by the thermal resistance of the package and adding the ambient temperature to the result.

$$T_J = (P_D \times \theta_{JA}) + T_A$$

FACTORS AFFECTING θ_{JA}

There are several factors which affect the thermal resistance of any IC package. Effective thermal management demands a sound understanding of all these variables. Package variables include the leadframe design and materials, the plastic used to encapsulate the device, and to a lesser extent other variables such as the die size and die attach methods. Other factors that have a significant impact on the θ_{JA} include the substrate upon which the IC is mounted, the density of the layout, the air-gap between the package and the substrate, the number and length of traces on the board, the use of thermally conductive epoxies, and external cooling methods.

PACKAGE CONSIDERATIONS

Studies with dual-in-line plastic (DIP) packages over the years have shown the value of proper leadframe design in achieving minimum thermal resistance. SMD leadframes are smaller than their DIP counterparts (see Figures 1a and 1b). Because the same die is used in each of the packages, the die-pad, or flag, must be at least as large in the SO as in the DIP.

While the size and shape of the leads have a measurable effect on θ_{JA}, the design factors that have the most significant effect are the die-pad size and the tie-bar size. With design constraints caused by both miniaturization and the need to assemble packages in an automated environment, the internal design of an SMD is much different than in a DIP. However, the design is one that strikes a balance between the need to miniaturize, the need to automate the assembly of the package, and the need to obtain optimum thermal characteristics.

LEAD FRAME MATERIAL is one of the more important factors in thermal management. For years the DIP leadframes were constructed out of Alloy-42. These leadframes met the producers' and users' specifications in quality and reliability. However three to five years ago, the leadframe material of DIPs was changed from Alloy-42 to Copper (CLF) in order to provide reduced θ_{JA} and extend the reliable temperature-operating range. While this change has already taken place for the DIP, it is still taking place for the SO package. Signetics began making 14-pin SO packages with CLF in April 1984 and completed conversion to CLF for all SO packages by 1985. As is shown in Figures 10 through 14, the change to CLF is producing dramatic results in the θ_{JA} of SO packages. All PLCCs are assembled with copper leadframes.

The MOLDING COMPOUND is another factor in thermal management. The compound used by Signetics and Philips is the same high purity epoxy used in DIP packages (at present, HC-10, Type II). This reduces corrosion caused by impurities and moisture.

OTHER FACTORS often considered are the die size, die attach methods, and wire bonding. Tests have shown that die size has a minor effect on θ_{JA} (see Figures 10 through 14).

While there is a difference between the thermal resistance of the silver-filled adhesive used for die attach and a gold silicon eutectic die attach, the thickness of this layer (1 – 2 mils) is so small as to make the difference insignificant.

Gold wire bonding in the range of 1.0 to 1.3 mils does not provide a significant thermal path in any package.

In summary, the SMD leadframe is much smaller then in a DIP and, out of necessity, is designed differently; however, the SMD package offers an adequate θ_{JA} for all moderate power devices. Further, the change to CLF will reduce the θ_{JA} even more, lowering the T_J and providing an even greater margin of reliability.

SIGNETICS' THERMAL RESISTANCE MEASUREMENTS — SMD PACKAGES

The graphs illustrated in this application note show the thermal resistance of Signetics' SMD devices. These graphs give the relationship between θ_{JA} (junction-to-ambient) or θ_{JC} (junction-to-case) and the device die size. Data is also provided showing the difference between still air (natural convection cooling) and air flow (forced cooling) ambients. All θ_{JA} tests were run with the SMD device soldered to test boards (See the Test Ambient section for details). It is important to recognize that the test board is an essential part of the test environment and that boards of different sizes, trace layouts or compositions may give different results from this data. Each SMD user should compare their system to the Signetics test system and determine if the data is appropriate or needs adjustment for their application.

Test Method

Signetics uses what is commonly called the TSP (temperature sensitive parameter) method. This method meets MIL-STD 883C, Method 1012.1. The basic idea of this method is to use the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power dissipation. The thermal resistance can be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{T_J - T_A}{P_D}$$

Test Procedure

TSP Calibration

The TSP diode is calibrated using a constant temperature oil bath and constant current power supply. The calibration temperatures used are typically 25°C and 75°C and are measured to an accuracy of ±0.1°C. The calibration current must be kept low to avoid significant junction heating, data given in this report used constant currents of either 1.0mA or 3.0mA. The temperature coefficient (K-Factor) is calculated using the following equation:

$$K = \left.\frac{T_2 - T_1}{V_{F2} - V_{F1}}\right| \quad I_F = \text{Constant}$$

Where: K = Temperature Coefficient (°C/mV)
T_2 = Higher Test Temperature (°C)
T_1 = Lower Test Temperature (°C)
V_{F2} = Forward Voltage at I_F and T_2
V_{F1} = Forward Voltage at I_F and T_1
I_F = Constant Forward Measurement Current
(See Figure 2)

Thermal Resistance Measurement

The thermal resistance is measured by applying a sequence of constant current and constant voltage pulses to the device under test. The constant current pulse (same current at which the TSP was calibrated) is used to measure the forward voltage of the TSP. The constant voltage pulse is used to heat the part. The measurement pulse is very short

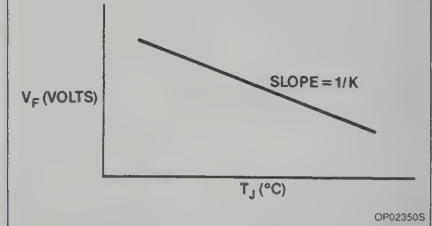


Figure 2. Forward Voltage — Junction Temperature Characteristics of a Semiconductor Junction Operating at a Constant Current. The K Factor is the Reciprocal of the Slope

(less than 1% of cycle) compared to the heating pulse (greater than 99% of cycle) to minimize junction cooling during measurement. This cycle starts at ambient temperature and continues until steady-state conditions are reached. The thermal resistance can then be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{K\ (V_{FA} - V_{FS})}{V_H \times I_H}$$

Where: V_{FA} = Forward Voltage of TSP at Ambient Temperature (mV)
V_{FS} = Forward Voltage of TSP at Steady-State Temperature (mV)
V_H = Heating Voltage (V)
I_H = Heating Current (A)

Test Ambient

θ_{JA} Tests

All θ_{JA} test data collected in this application note was obtained with the SMD devices soldered to either Philips SO Thermal Resistance Test Boards or Signetics PLCC Thermal Resistance Test Boards with the following parameters:

Board size
- SO Small: 1.12″ × 0.75″ × 0.059″
- SO Large: 1.58″ × 0.75″ × 0.059″
- PLCC: 2.24″ × 2.24″ × 0.062″

Board Material - Glass epoxy, FR-4 type with 1 oz. sq.ft. copper solder coated

Board Trace Configuration - See Figure 3.

SO devices are set at 8 – 9 mil stand-off and SO boards use one connection pin per device lead. PLCC boards generally use 2 – 4 connection pins regardless of device lead count. Figure 5 shows a cross-section of an SO part soldered to test board and Figure 4 shows typical board/device assemblies ready for θ_{JA} Test.

The still air tests were run in a box having a volume of 1 cubic foot of air at room temperature. The air flow tests were run in a 4″ × 4″ cross-section by 26″ long wind tunnel with air at room temperature. All devices were soldered on test boards and held in a horizontal test position. The test boards were held in a Textool ZIF socket with 0.16″ stand-off. Figure 6 shows the air flow test setup.

θ_{JC} Tests

The θ_{JC} test is run by holding the test device against an "infinite" heat sink (water cooled block approximately 4″ × 7″ × 0.75″) to give a θ_{CA} (case-to-ambient) approaching zero. The copper heat sink is held at a constant temperature (≈20°C) and monitored with a thermocouple (0.040″ diameter sheath, grounded junction type K) mounted flush with heat sink surface and centered below die in the test device. Figure 7 shows the θ_{JC} test mounting for a PLCC device.

SO devices are mounted with the bottom of the package held against the heat sink. This is achieved by bending the device leads straight out from the package body. Two small wires are soldered to the appropriate leads for tester connection. Thermal grease is used between the test device and heat sink to assure good thermal coupling.

PLCC devices are mounted with the top of the package held against the heat sink. A small spacer is used between the hold-down mechanism and PLCC bottom pedestal. Small hook up wires and thermal grease are used as with the SO setup. Figure 7 shows the PLCC mounting.

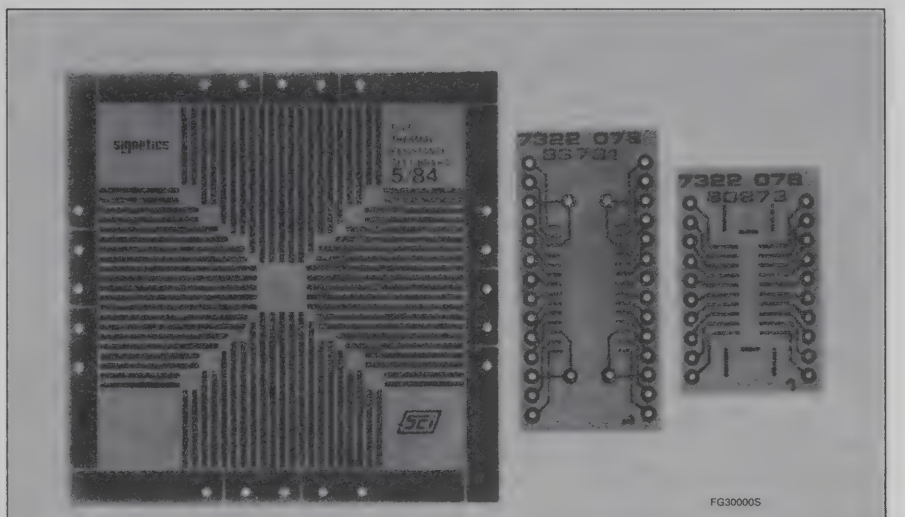


Figure 3. Board Trace Configuration for Thermal Resistance Test Boards

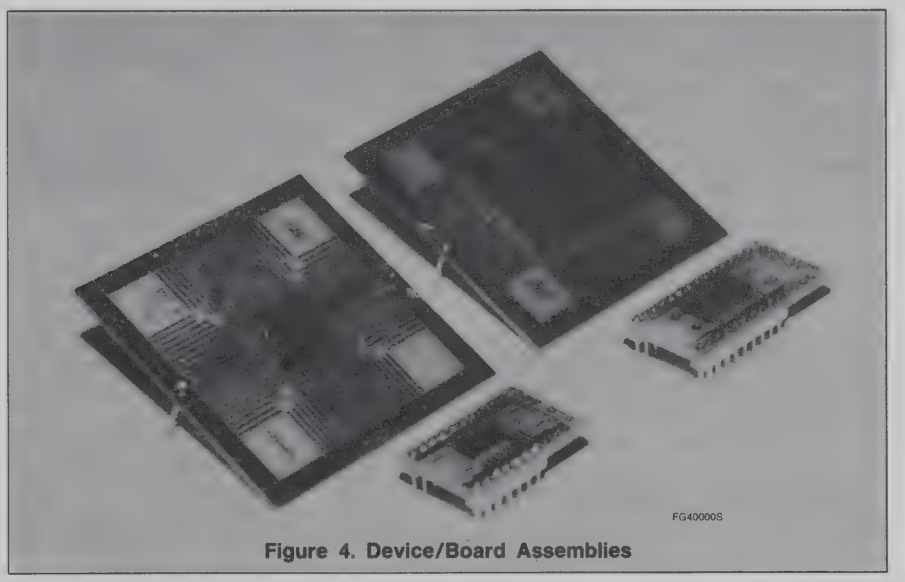


Figure 4. Device/Board Assemblies

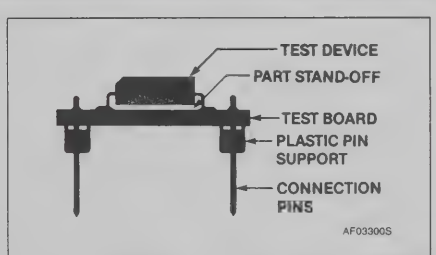
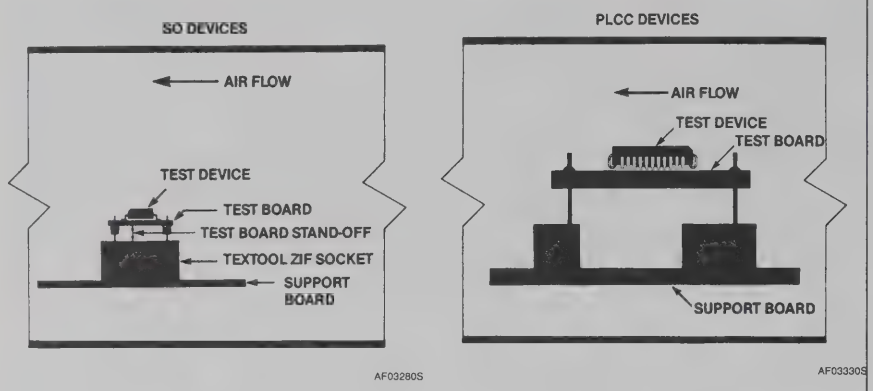


Figure 5. Cross-Section of Test Device Soldered to Test Board



SO Devices PLCC Devices

Figure 6. Air Flow Test Setup

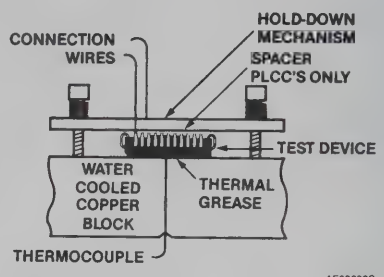


Figure 7. θ_{JC} Test Setup With PLCC Device

DATA PRESENTATION

The data presented in this application note was run at constant power dissipation for each package type. The power dissipation used is given under Test Conditions for each graph. Higher or lower power dissipation will have a slight effect on thermal resistance. The general trend of thermal resistance decreasing with increasing power is common to all packages. Figure 8 shows the average effect of power dissipation on SMD θ_{JA}.

Thermal resistance can also be affected by slight variations in internal leadframe design such as pad size. Larger pads give slightly lower thermal resistance for the same size die. The data presented represents the typical Signetics leadframe/die combinations with large die on large pads and small die on small pads. The effect of leadframe design is within the ±15% accuracy of these graphs.

SO devices are currently available in both copper or alloy 42 leadframes; however, Signetics is converting to copper only. PLCC devices are only available using copper leadframes.

The average lowering effect of air flow on SMD θ_{JA} is shown in Figure 9.

Thermal Calculations

The approximate junction temperature can be calculated using the following equation:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

Where: T_J = Junction Temperature (°C)
θ_{JA} = Thermal Resistance Junction-to-Ambient (°C/W)
P_D = Power Dissipation at a T_J ($V_{CC} \times I_{CC}$) (W)
T_A = Temperature of Ambient (°C)

Example: Determine approximate junction temperature of SOL-20 at 0.5W dissipation using 10,000 sq. mil die and copper leadframe in still air and 200 LFPM air flow ambients. Given $T_A = 30°C$,

1. Find θ_{JA} for SOL-20 using 10,000 sq. mil die and copper leadframe from typical θ_{JA} data —SOL-20 graph.
   Answer: 88°C/W @ 0.7W
2. Determine θ_{JA} @ 0.5W using Average Effect of Power Dissipation on AMD θ_{JA}, Figure 8.

   Percent change in Power =

   $$\frac{0.5W - 0.7W}{0.7W} \times 100 = -28.6\%$$

   From Figure 8:
   28.6% change in power gives 3.5% increase in θ_{JA}
   Answer:
   88°C/W + (88 × 0.035) = 91°C/W @ 0.5W
3. Determine θ_{JA} @ 0.5W in 200 LFPM air flow from Average Effect of Air Flow on SMD θ_{JA}, Figure 9.
   From Figure 9:
   200 LFPM air flow gives 14% decrease in θ_{JA}
   Answer:
   91°C/W – (91 × 0.14) = 78°C/W
4. Calculate approximate junction temperature
   Answer:
   T_J (still air) = (91°C/W × 0.5W) + 30 = 76°C
   T_J (200 LFPM) = (78°C/W × 0.5W) + 30 = 69°C

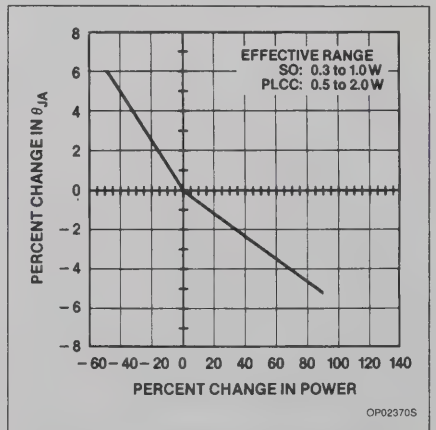


Figure 8. Average Effect of Power Dissipation on SMD θ_{JA}

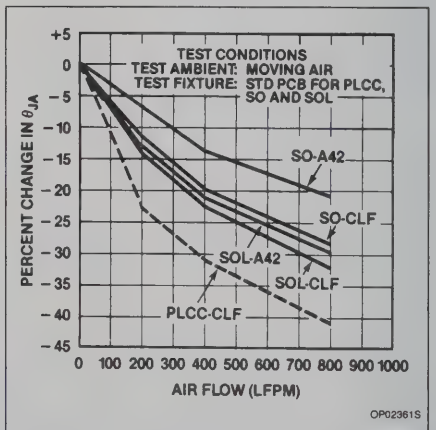
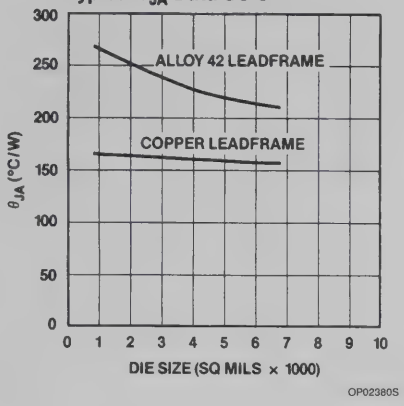


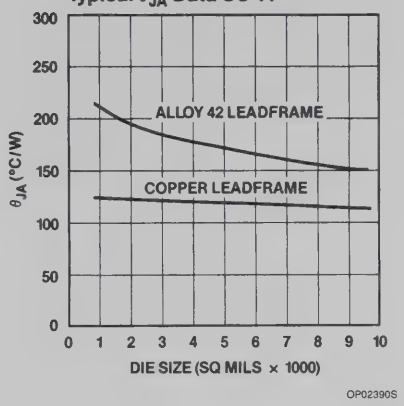
Figure 9. Average Effect of Air Flow on SMD θ_{JA}

TYPICAL SMD THERMAL (θ_{JA})

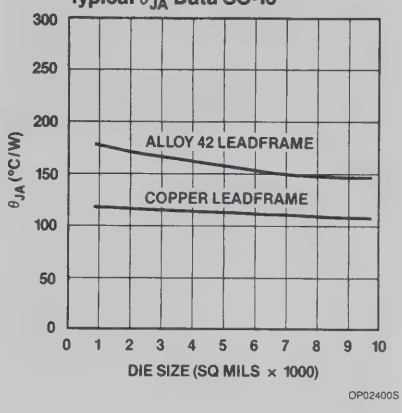
Typical θ_{JA} Data SO-8[1]



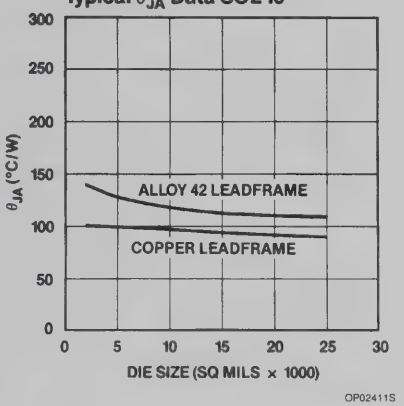
Typical θ_{JA} Data SO-14[1]



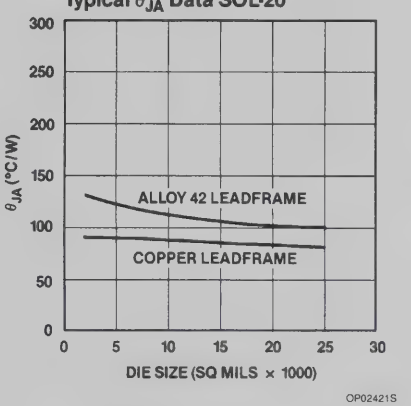
Typical θ_{JA} Data SO-16[1]



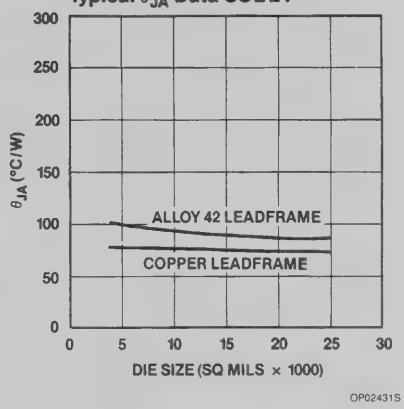
Typical θ_{JA} Data SOL-16[2]



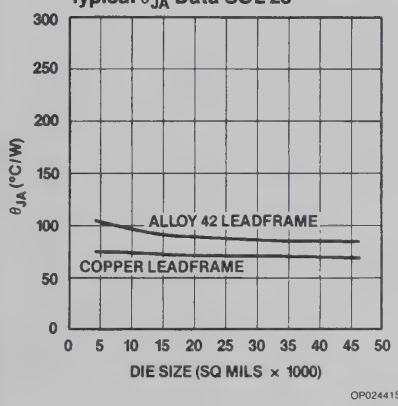
Typical θ_{JA} Data SOL-20[3]



Typical θ_{JA} Data SOL-24[3]



Typical θ_{JA} Data SOL-28[3]



NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.12" × 0.75" × 0.059")
Accuracy:	±15%

2. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")
Accuracy:	±15%

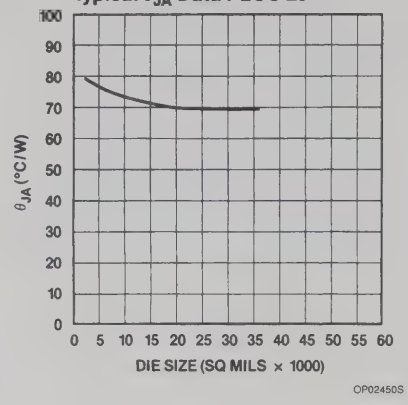
3. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.7W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")
Accuracy:	±15%

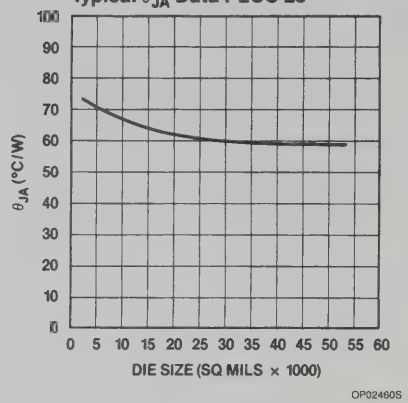
Figure 10

TYPICAL SMD THERMAL (θ_{JA})

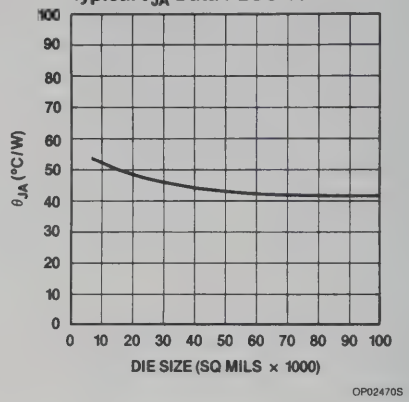
Typical θ_{JA} Data PLCC-20[1]



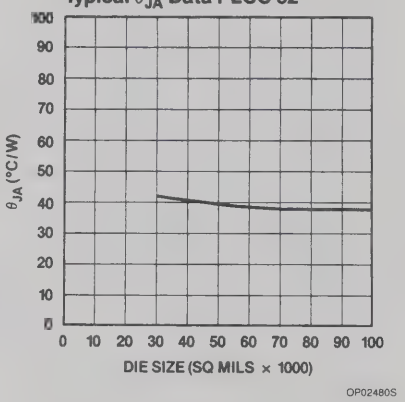
Typical θ_{JA} Data PLCC-28[1]



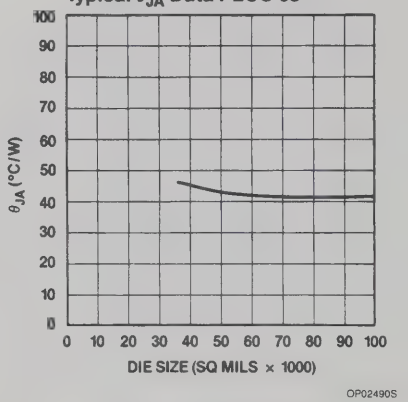
Typical θ_{JA} Data PLCC-44[1]



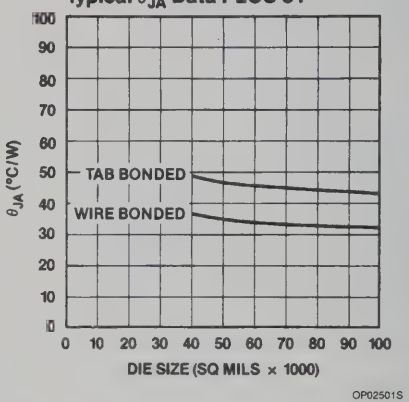
Typical θ_{JA} Data PLCC-52[1]



Typical θ_{JA} Data PLCC-68[2]



Typical θ_{JA} Data PLCC-84[3]



NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

2. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

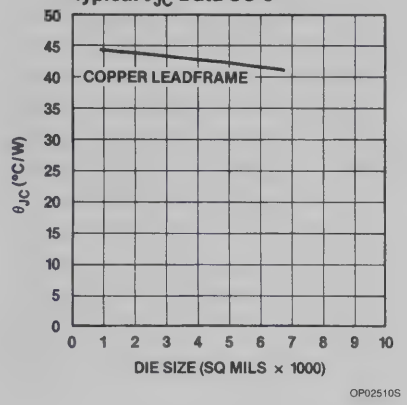
3. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	1.5W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

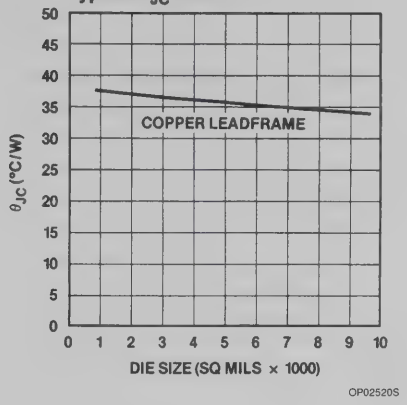
Figure 11

TYPICAL SMD THERMAL (θ_{JC})

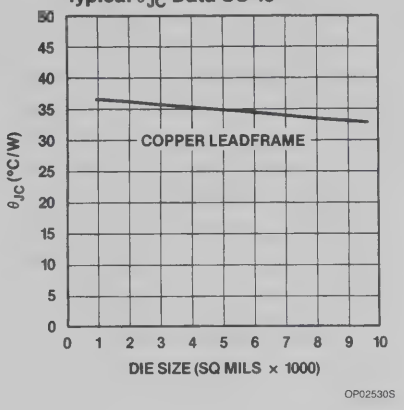
Typical θ_{JC} Data SO-8 [1]



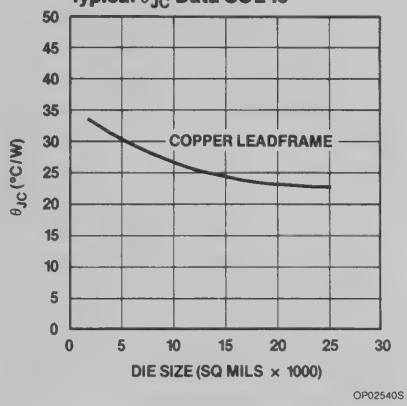
Typical θ_{JC} Data SO-14 [1]



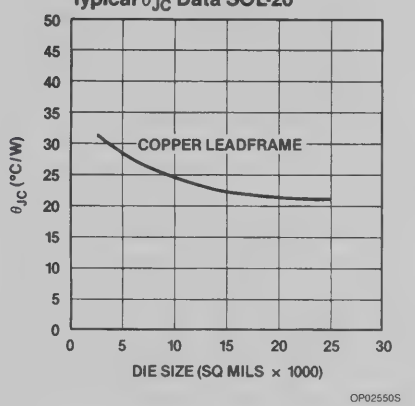
Typical θ_{JC} Data SO-16 [1]



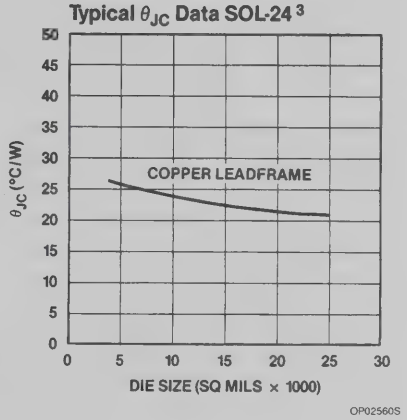
Typical θ_{JC} Data SOL-16 [1]



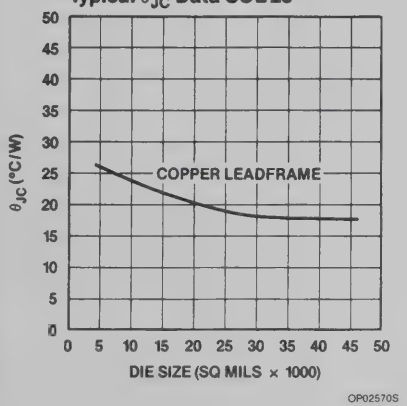
Typical θ_{JC} Data SOL-20 [2]



Typical θ_{JC} Data SOL-24 [3]



Typical θ_{JC} Data SOL-28 [3]



NOTES:

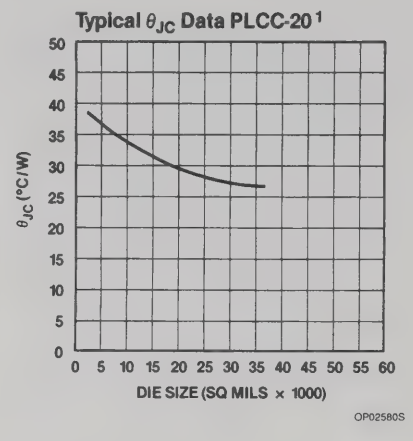
1. TEST CONDITIONS:
Power dissipation: 0.5W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

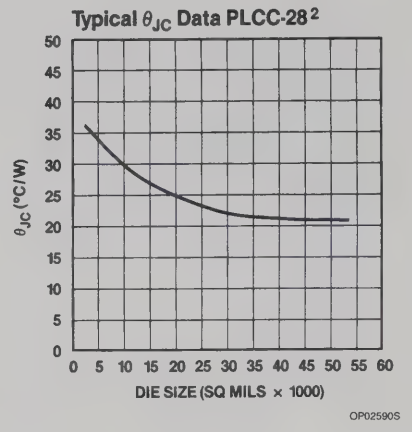
2. TEST CONDITIONS:
Power dissipation: 0.7W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

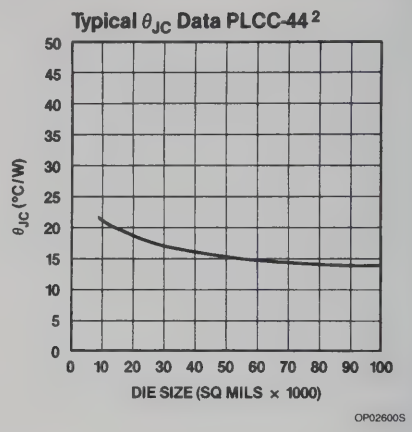
3. TEST CONDITIONS:
Power dissipation: 1.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

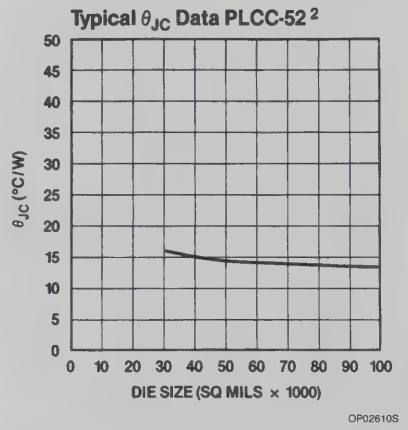
Figure 12

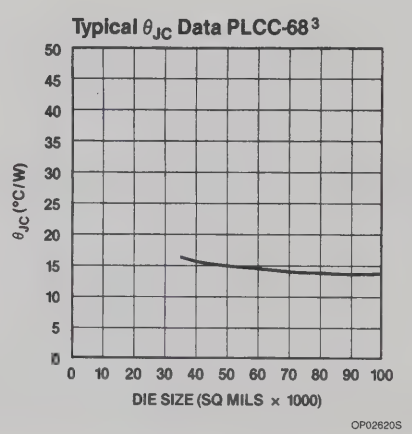
TYPICAL SMD THERMAL (θ_{JC})

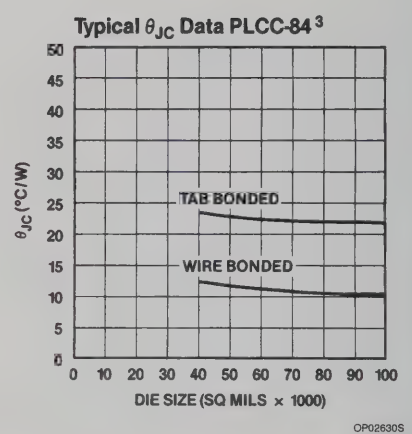












NOTES:

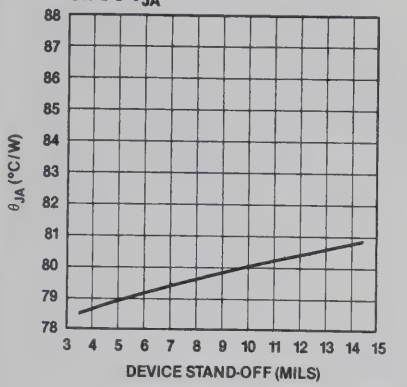
1. TEST CONDITIONS:
Power dissipation: 0.75W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

2. TEST CONDITIONS:
Power dissipation: 1.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

3. TEST CONDITIONS:
Power dissipation: 2.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

Figure 13

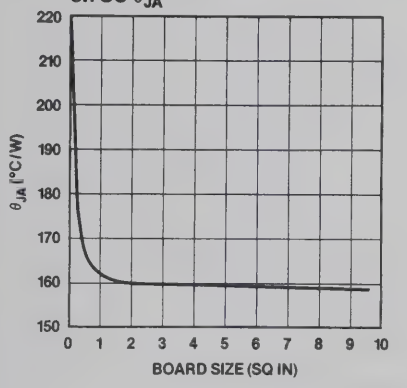
Effect of Device Stand-Off on SO θ_{JA}[1]



NOTES:
1. TEST CONDITIONS:

Package type:	SOL-20 CLF
Die size:	11,322 sq mils
Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Philips PCB (1.58″ × 0.75″ × 0.059″)

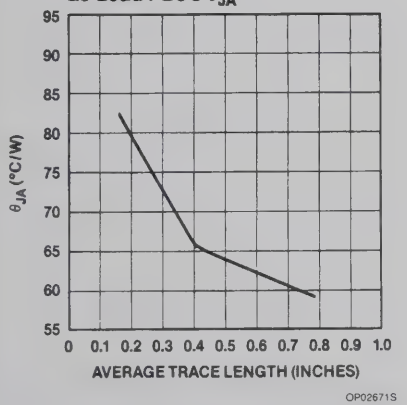
Effect of Board Size on SO θ_{JA}[2]



2. TEST CONDITIONS:

Package type:	SO-14 CLF
Die size:	5,040 sq mils
Test ambient:	Still air
Power dissipation:	0.6W
Test fixture:	0.062″ thick PCB with "No Traces" 8-9 MIL stand-off

Effect of Trace Length on 28-Lead PLCC θ_{JA}[3]



3. TEST CONDITIONS:

Package type:	PLCC-28 CLF
Die size:	10,445 sq mils
Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″) trace 27 MIL wide 1 oz SQ ft copper

Figure 14

SYSTEM CONSIDERATIONS

With the increases in layout density resulting from surface mounting with much smaller packages, other factors become even more important. THE USER IS IN CONTROL OF THESE FACTORS.

One of the most obvious factors is the substrate material on which the parts are mounted. Environmental constraints, cost considerations and other factors come into play when choosing a substrate. The choice is expanding rapidly, from the standard glass epoxy PWB materials and ceramic substrates to flexible circuits, injection molded plastics, and coated metals. Each of these has its own thermal characteristics which must be considered when choosing a substrate material.

Studies have shown that the air gap between the bottom of the package and the substrate has an effect on θ_{JA}. The larger the gap, the higher the θ_{JA}. Using thermally conductive epoxies in this gap can slightly reduce the θ_{JA}.

It has long been recognized that external cooling can reduce the junction temperatures of devices by carrying heat away from both the devices and the board itself. Signetics has done several studies on the effects of external cooling on boards with SO packages. The results are shown in Figures 15 through 18.

The designer should avoid close spacing of high power devices so that the heat load is spread over as large an area as possible. Locate components with a higher junction temperature in the cooler locations on the PCBs.

The number and size of traces on a PWB can affect θ_{JA} since these metal lines can act as radiators, carrying heat away from the package and radiating it to the ambient. Although the chips themselves use the same amount of energy in either a DIP or an SO package, the increased density of a Surface Mounted Assembly concentrates the thermal energy into a smaller area.

It is evident that nothing is free in PWB layout. More heat concentrated into a smaller area makes it incumbent on the system designer to provide for the removal of thermal energy from his system.

Large conductor traces on the PCB conduct heat away from the package faster than small traces. Thermal vias from the mounting surface of the PCB to a large area ground plane in the PCB reduces the heat buildup at the package.

In addition to the package's thermal considerations, thermal management requires one to at least be aware of potential problems caused by mismatch in thermal expansion.

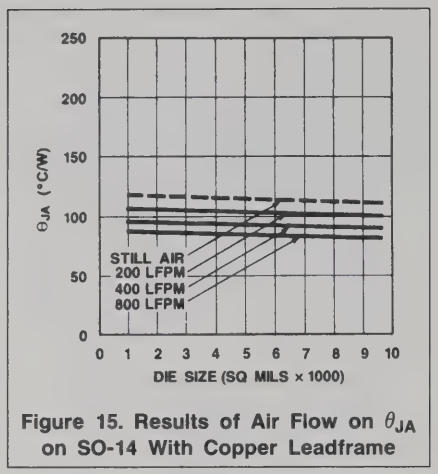


Figure 15. Results of Air Flow on θ_{JA} on SO-14 With Copper Leadframe

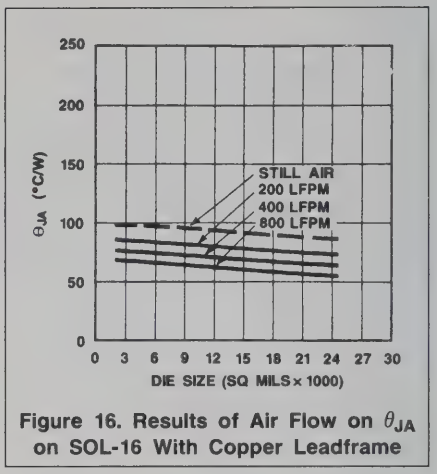


Figure 16. Results of Air Flow on θ_{JA} on SOL-16 With Copper Leadframe

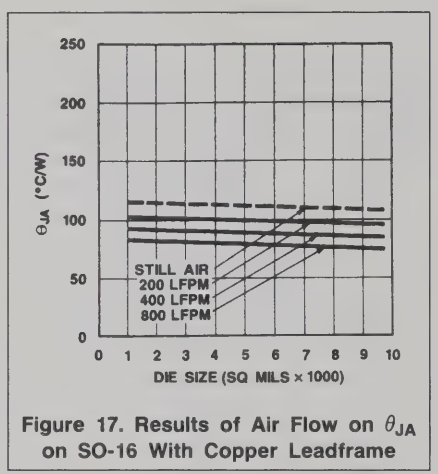


Figure 17. Results of Air Flow on θ_{JA} on SO-16 With Copper Leadframe

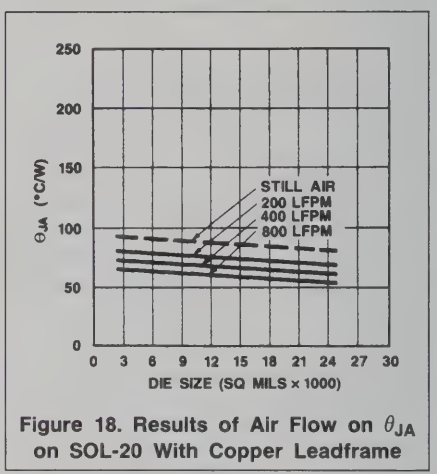


Figure 18. Results of Air Flow on θ_{JA} on SOL-20 With Copper Leadframe

The very nature of the SMD assembly, where the devices are soldered directly onto the surface, not through it, results in a very rigid structure. If the substrate material exhibits a different thermal coefficient of expansion (TCE) than the IC package, stresses can be setup in the solder joints when they are subjected to temperature cycling (and during the soldering process itself) that may ultimately result in failure.

Because some of the boards assembled will require the use of Leadless Ceramic Chip Carriers (LCCCs), TCE must be understood. As will be seen below, TCE is less of a problem with the commercial SMD packages with leads.

Take the example of a leadless ceramic chip carrier with a TCE of about 6×10^{-6}/K soldered to a conventional glass-epoxy laminate with a TCE in the region of 16×10^{-6}/K. This thermal expansion mismatch has been shown to fracture the solder joints during thermal cycling. Substrate materials with matched TCEs should be evaluated for these SMD assemblies to avoid problems caused by thermal expansion mismatch.

The stress level associated with thermal expansion and contraction of small SMDs such as capacitors and resistors, where the actual change in length is small, are normally rather low. However, as component sizes increase, stresses can increase substantially.

Thermal expansion mismatch is unlikely to cause too many problems in systems operating in benign environments; but, in harsher conditions, such as thermal cycling in military or avionic applications, the mechanical stresses setup in solder joints due to the different TCEs of the substrate and the component are likely to cause failure.

The basic problem is outlined in Figure 19. The leadless SMD is soldered to the substrate as shown, resulting in a very rigid structure. If the substrate material exhibits a different TCE from that of the SMD material, the amount of expansion for each will differ for any given increase in temperature. The soldered joint will have to accommodate this difference, and failure can ultimately result. The larger the component size, the higher the stress levels so that this phenomenon is at its most critical in applications requiring large LCCCs with high pin-counts.

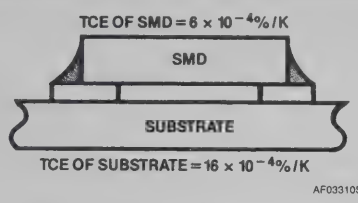


Figure 19. The Basic Problem of Thermal Expansion Mismatch Is That the Substrate and Component May Each Have Different Thermal Coefficients of Expansion.

NOTE: Data provided by N.V. Philips

To address this problem, three basic solutions are emerging. First, the use of leadless ceramic chip carriers can sometimes be avoided by using leaded devices; the leads can flex and absorb the stress. Second, when this solution is not feasible, the stresses can be taken up by inserting a compliant elastomeric layer between the ceramic package and the epoxy glass substrate. Third, TCE values of component and substrate can be matched.

USING LEADED DEVICES (SO, SOL & PLCC)

The current evolution in commercial electronics includes the adoption of the commercial SMD packages, i.e. SO with gull-wing leads or the PLCC with rolled-under J-leads, rely on the compliance of the leads themselves to avoid any serious problems of thermal expansion mismatch. At elevated temperatures, the leads flex slightly and absorb most of the mechanical stress resulting from the thermal expansion differentials.

Similarly, leaded holders can be used with LCCCs to attach them to the substrate and thus absorb the stress.

Unfortunately, using a lead does not always ensure sufficient compliancy. The material from which the lead is made, and the way it is formed and soldered can adversely affect it. For example, improper soldering techniques, which cause excess solder to over-fill the bend of the gull-wing lead of an SO can significantly reduce the lead's compliancy.

COMPLIANT LAYER

This approach introduces a compliant layer onto the interface surface of the substrate to absorb some of the stresses. A 50μm thick elastomeric layer is bonded to the laminate. To make contacts, carbon or metalic powders are introduced to form conductive stripes in the nonconductive elastomer material. Unfortunately, substrates using this technique are substantially more expensive than standard uncoated boards.

Another solution is to increase the compliancy of the solder joint. This is done by increasing the stand-off height between the underside of the component and the substrate. To do this, a solder paste containing lead or ceramic spheres which do not melt when the surrounding solder reflows, thus keeping the component above the substrate can be used.

MATCHING TCE

There are two ways to approach this solution. The TCE of the substrate laminate material can be matched to that of the LCCC either by replacing the glass fibers with fibers exhibiting a lower TCE (composites such as epoxy-Kevlar® or polyimide-Kevlar and polyimide-quartz), or by using low TCE metals (such as Invar®, Kovar, or molybdenum).

This latter approach involves bonding a glass-polyimide or a glass-epoxy multilayer to the low TCE restraining core material. Typical of such materials are copper-Invar-copper, Alloy-42, copper-molybdenum-copper, and copper-graphite. These restraining-core constructions usually require that the laminate be bonded to both sides to form a balanced structure so that they will not warp or twist.

This inevitably means an increase in weight, which has always been a negative factor in this approach. However, the SMD substrate can be smaller and the components more densely packed in many cases overcoming the weight disadvantages. On the positive side, the material's high thermal conductivity helps to keep the components cool. Moreover, copper-clad-Invar lends itself readily to moisture-proof multilayering for the creation of ground and power planes and for providing good inherent EMI/RFI shielding.

Kevlar is lighter and widely used for substrates in military applications; but, it suffers from a serious drawback which, although overcome to a certain extent by careful attention to detail, can cause problems. The material, when laminated, can absorb moisture and chemical processing fluids around the edges. Thermal conductivity, machinability and cost are not as attractive as for copper-clad Invar.

For the majority of commercial substrates however, where the use of ceramic chip carriers in any quantity is the exception rather than the rule, and when adequate cooling is available, the mismatch of TCEs poses little or no problem. For these substrates traditional FR-4 glass-epoxy and phenolic-paper will no doubt remain the most widely used materials.

Although FR-4 epoxy-glass has been the traditional material for plated-through professional substrates, it is phenolic-paper laminate (FR-2) which finds the widest use in consumer electronics. While it is the cheapest material, it unfortunately has the lowest dimensional stability, rendering it unsuitable for the mounting of LCCCs.

SUBSTRATE TYPES

FR-4 glass-epoxy substrates are the most commonly used for commercial electronic circuits. They have the advantage of being cheap, machinable, and lightweight. Substrate size is not limited. On the negative side, they have poor thermal conductivity and a high TCE, between 13 and 17 $\times 10^{-6}$/K. This means they are a poor match to ceramic.

Glass polyimide substrates have a similar TCE range to glass-epoxy boards, but better thermal conductivity. They are, however, three to four times more expensive.

Polyimide Kevlar substrates have the advantage of being lightweight and not restricted in size. Conventional substrate processing methods can be used and its TCE (between 4 and 8), matches that of ceramic. Its disadvantages are that it is expensive, difficult to drill and is prone to resin microcracking and water absorption.

Polyimide quartz substrates have a TCE between 6 and 12 making them a good match for LCCCs. They can be processed using conventional techniques, although drilling vias can be difficult. They have good dielectric properties and compare favorably with FR-4 for substrate size and weight.

Alumina (ceramic) substrates are used extensively for high-reliability military applications and thick-film hybrids. The weight, cost, limited substrate size and inherent brittleness of alumina means that its use as a substrate material is limited to applications where these disadvantages are outweighed by the advantage of good thermal conductivity and a TCE that exactly matches that of LCCCs. A further limitation is that they require Thick-film screening processing.

Copper-clad Invar substrates are the leading contenders for TCE control at present. It can be tailored to provide a selected TCE by varying the copper-to-Invar ratio. Figure 20 shows the construction of a typical multilayer substrate employing two cores providing the power and ground planes. Plated-through holes provide an integral board-to-board interconnection. The low TCE of the core dominates the TCE of the overall substrate, making it possible to mount LCCCs with confidence.

Because the TCE of copper is high, and that of Invar is low, the overall TCE of the substrate can be adjusted by varying the thickness of the copper layers. Figure 21 plots the TCE range of the copper-clad Invar as a function of copper thickness, and shows the TCE range of each of several other materials to which the clad material can be matched. For example, if the TCE of Alumina is to be matched, then the core should have about 46% thickness of copper. When this material is used as a thermal mounting plane, it also acts as a heatsink.

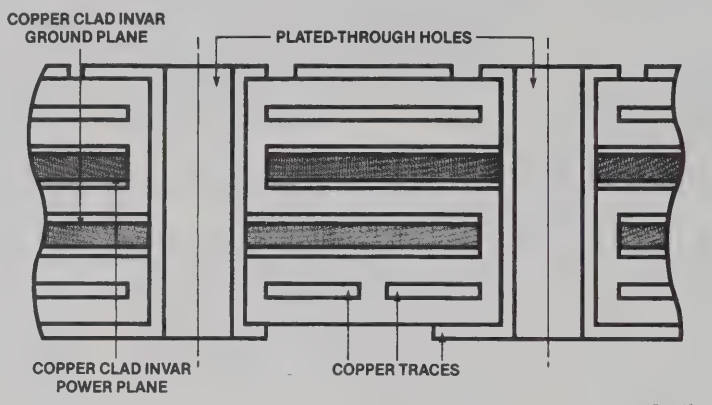


Figure 20. Section Through a Typical Multilayer Substrate Incorporating Copper-clad Invar Ground and Power Planes, Interconnected Via Plated-though Holes.

NOTE: Data provided by N.V. Philips

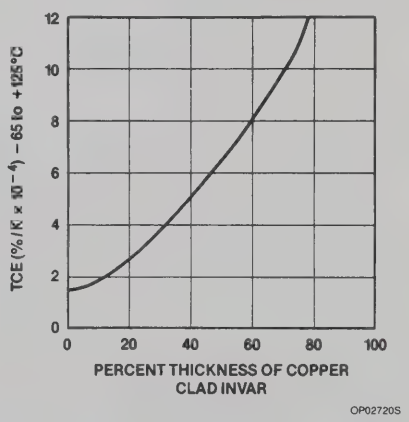


Figure 21. The TCE Range of Copper-clad Invar as a Function of Copper Thickness.

NOTE: Data provided by N.V. Philips

Table 1. Substrate Material Properties

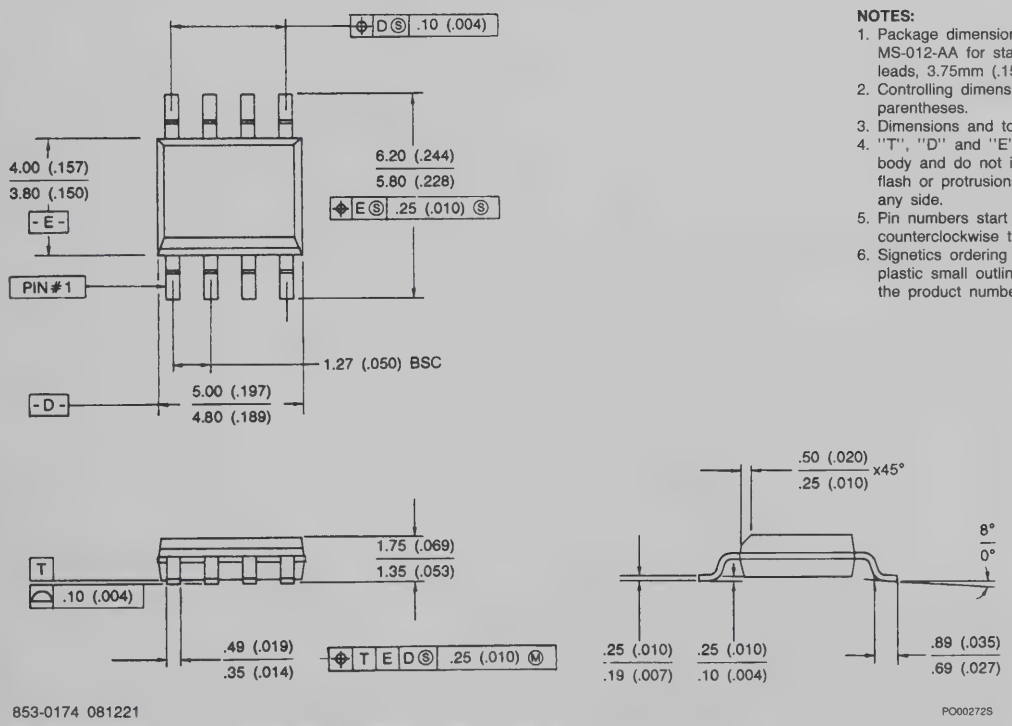
SUBSTRATE MATERIAL	TCE (10^{-6}/K)	THERMAL CONDUCTIVITY (W/m^{3}K)
Glass-epoxy (FR-4)	13 – 17	0.15
Glass polyimide	12 – 16	0.35
Polyimide Kevlar	4 – 8	0.12
Polyimide quartz	6 – 12	TBD
Copper-clad Invar	6.4 (typical)	165 (lateral) 16 (transverse)
Alumina	5 – 7	21
Compliant layer Substrate	See Notes	0.15 – 0.3

NOTES:
Compliant layer conforms to TCE of the LCCC and to base substrate material.
Data provided by N.V. Philips
KEVLAR® is a registered trademark of DU PONT.
INVAR® is a registered trademark of TEXAS INSTRUMENTS.

CONCLUSION

Thermal management remains a major concern of producers and users of ICs. The advent of SMD technology has made a thorough understanding of the thermal characteristics of both the devices and the systems they are used in mandatory. The SMD package, being smaller, does have a higher θ_{JA} than its standard DIP counterpart . . . even with Copper Lead Frames. That is the major trade-off one accepts for package miniaturization. However, consideration of all the variables affecting IC junction temperatures will allow the user to take maximum advantage of the benefits derived from use of this technology.

SO-8

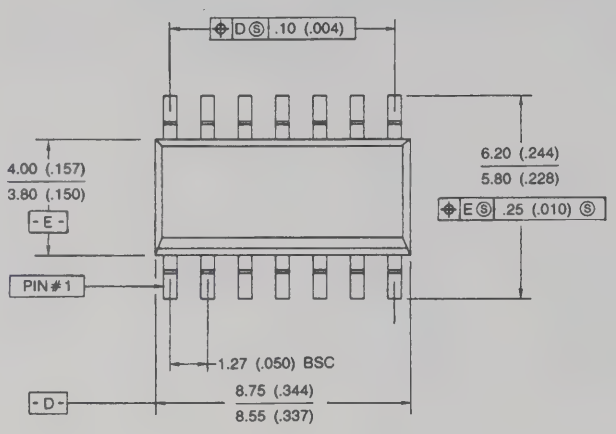


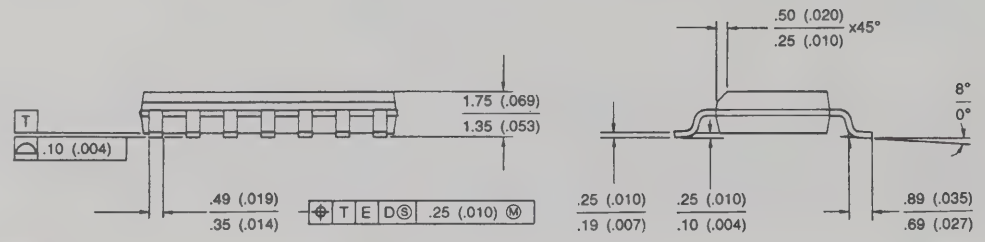
NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0174 081221

PO00272S

SO-14





NOTES:
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2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

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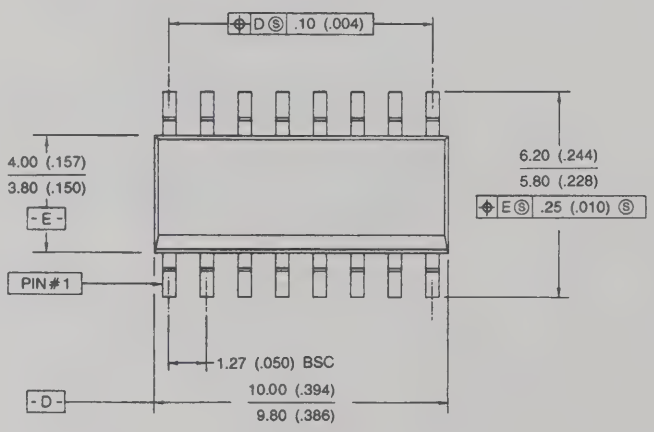
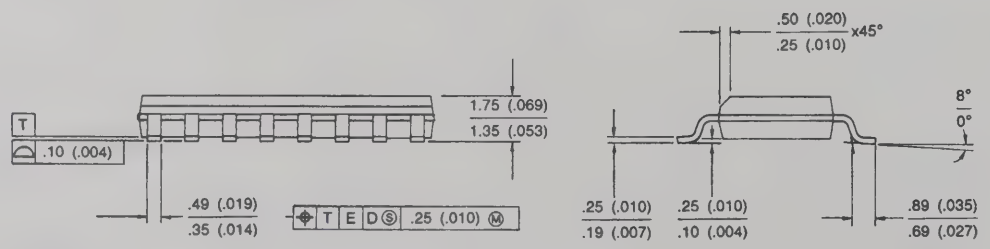
PO00262S

SO-16



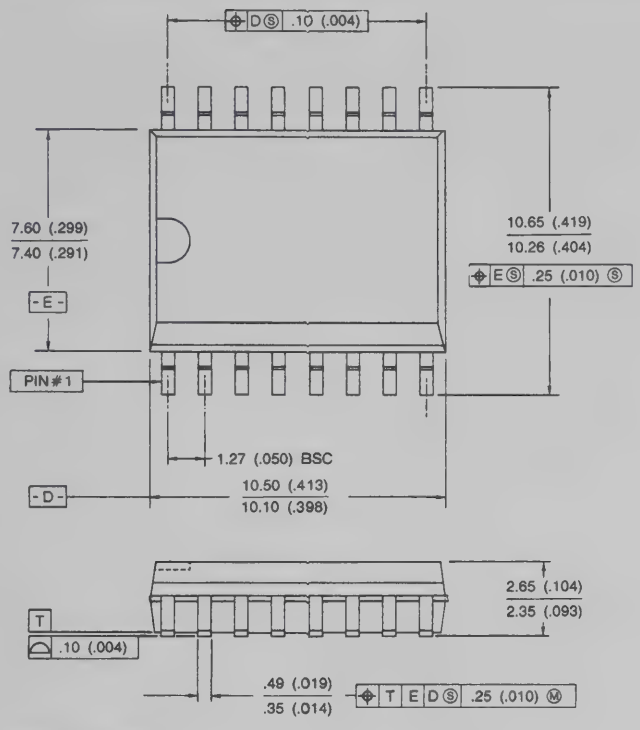


NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

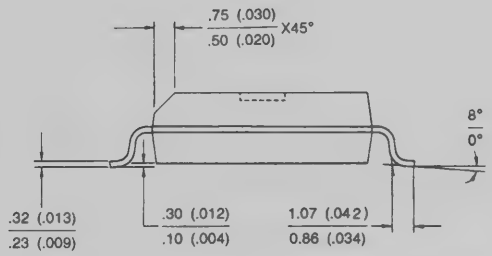
853-0005 081216

PO00251S

SOL-16



NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



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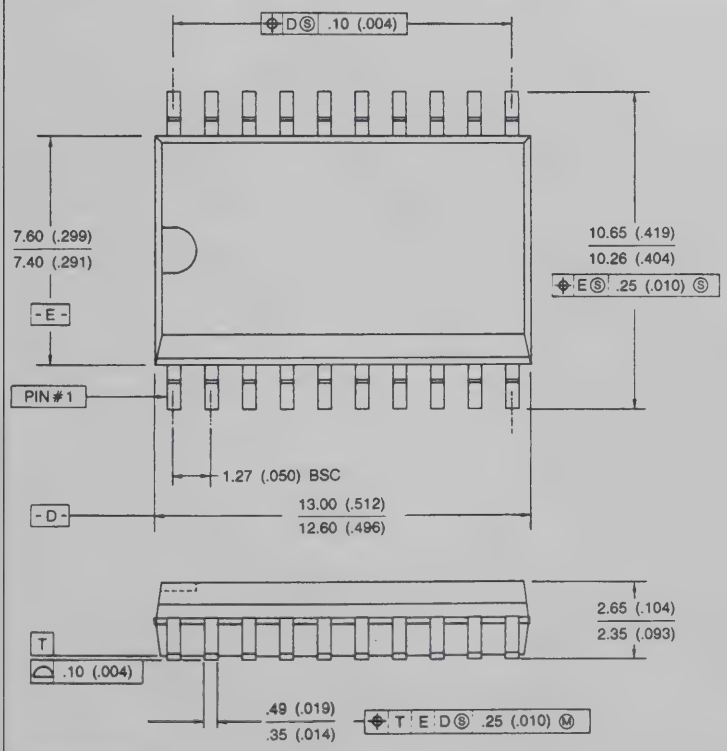
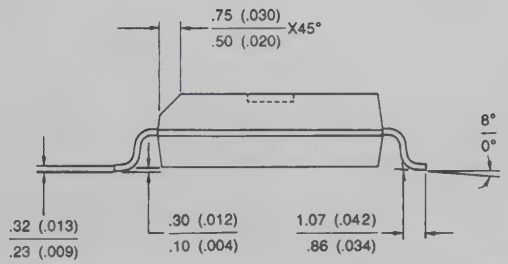
PO00241S

SOL-20



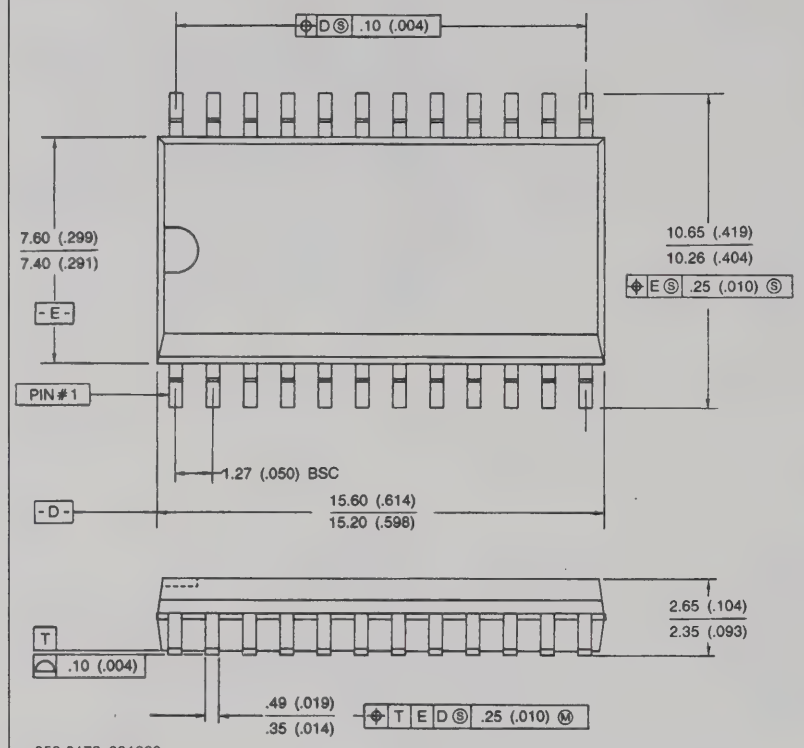
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

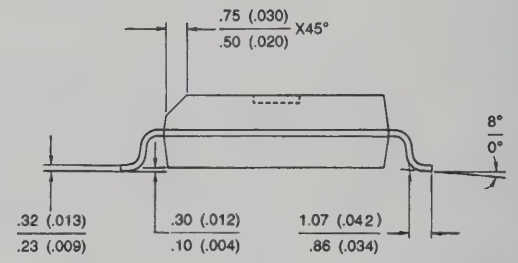


853-0172 081219

PO00231S

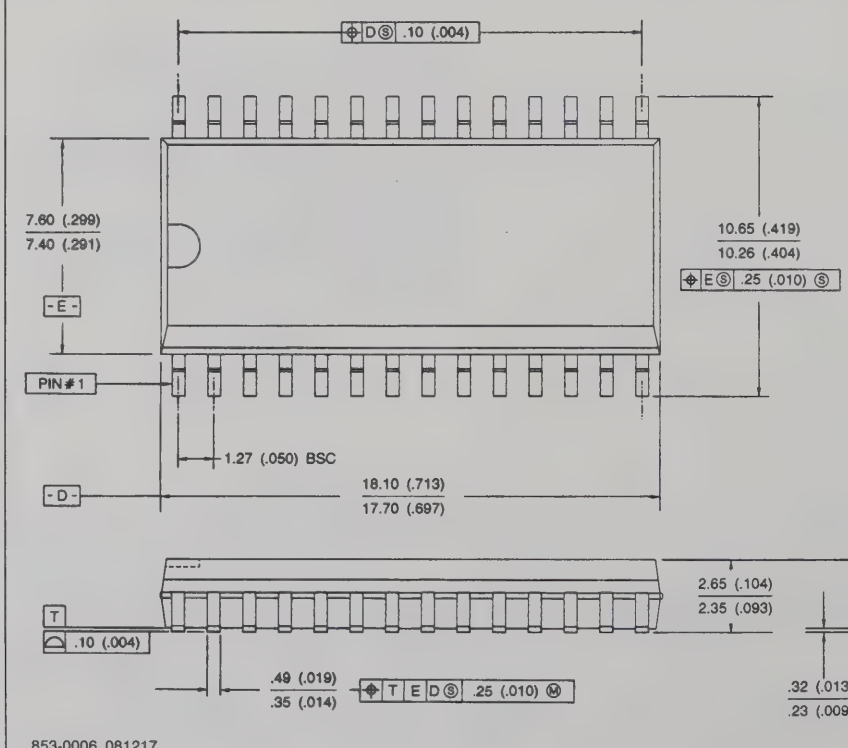
SOL-24

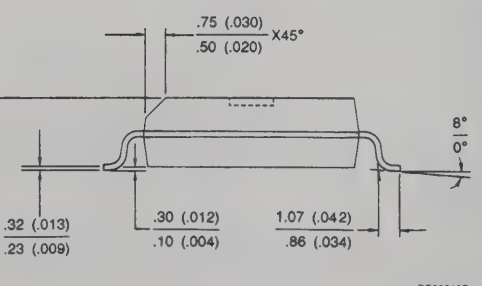




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

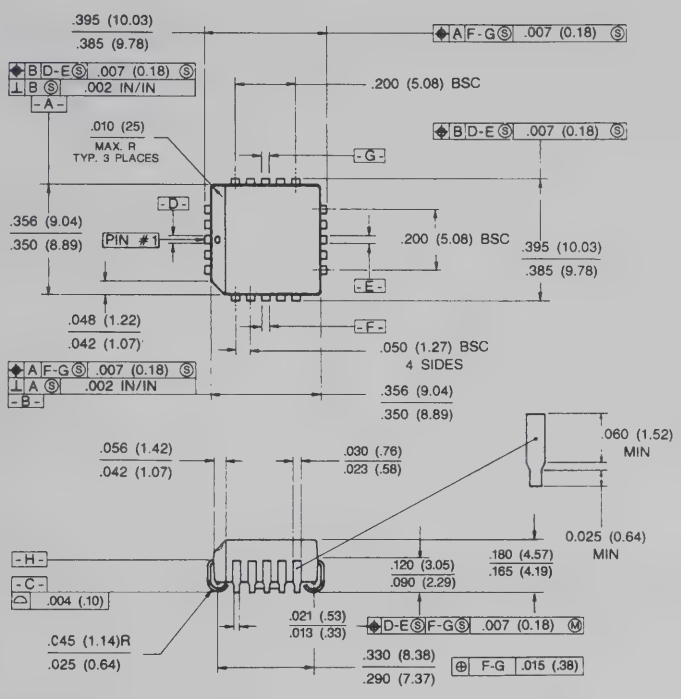
SOL-28

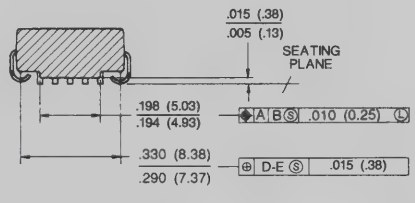




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

PLCC-20



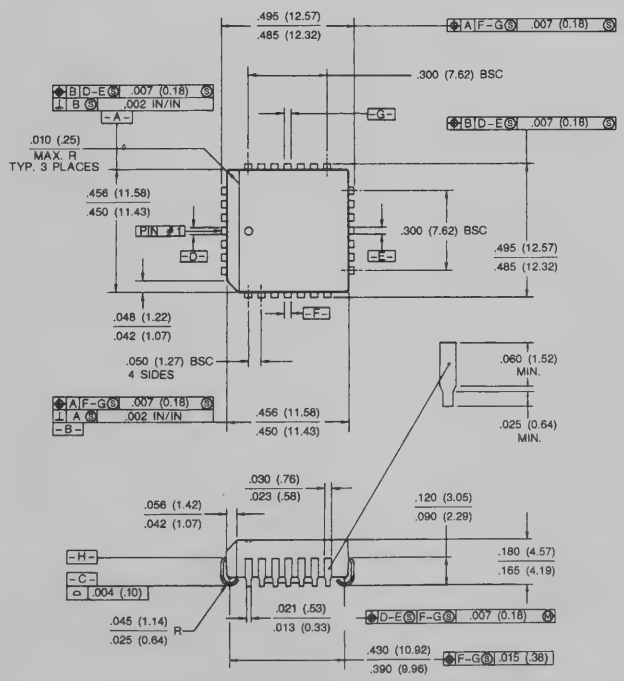


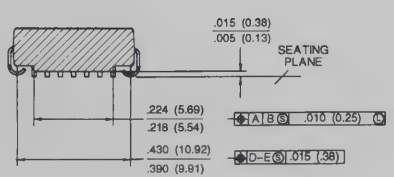
NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #20 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0400 081226

PO00632S

PLCC-28



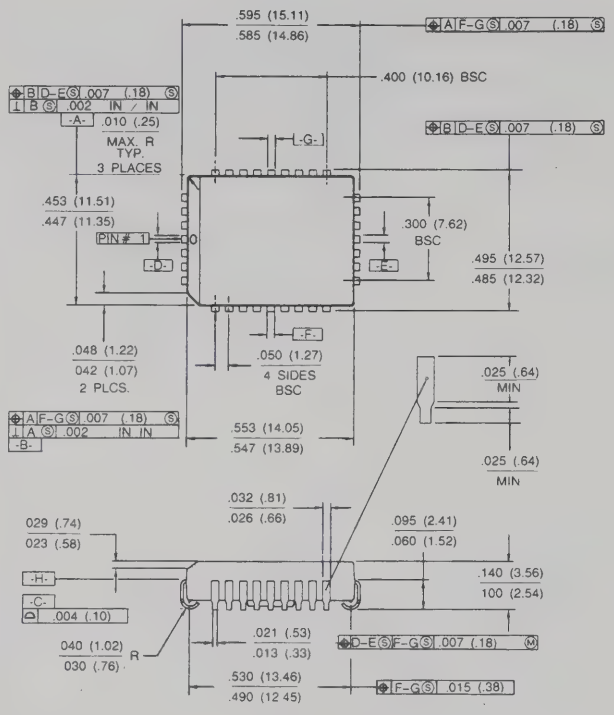


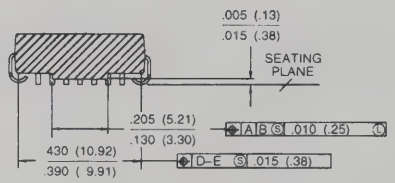
NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #28 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0401 081227

PO00612S

PLCC-32

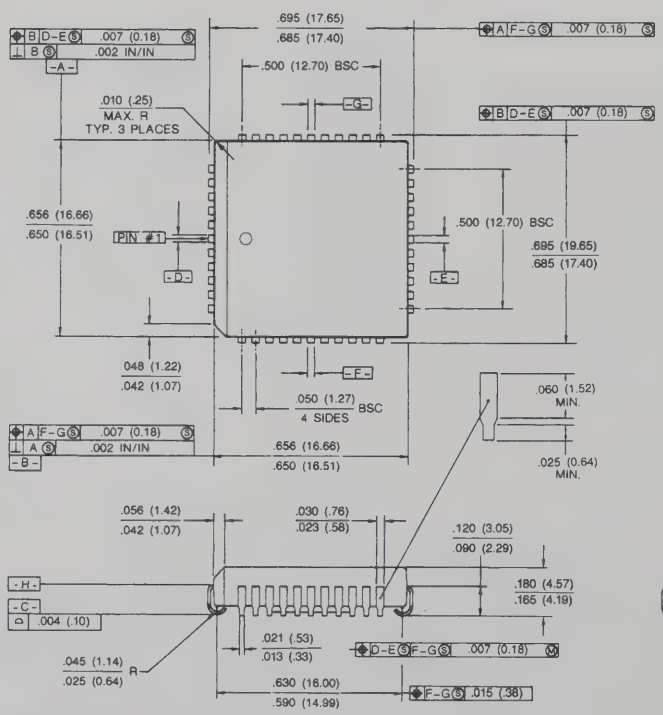


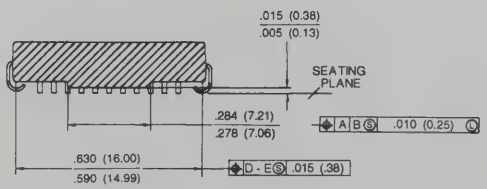


NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #28 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

PO00170S

PLCC-44



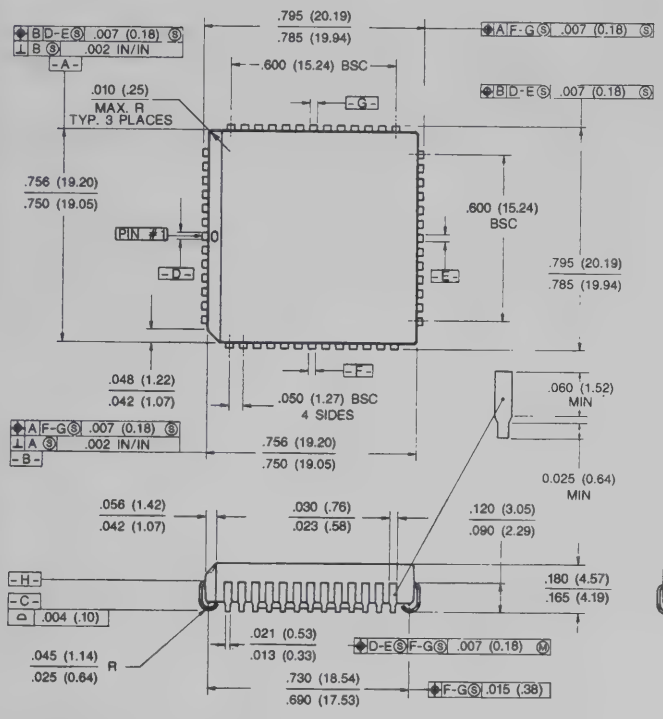


NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AL for plastic leaded chip carrier 44 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #44 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0403 081229

PO00602S

PLCC-52



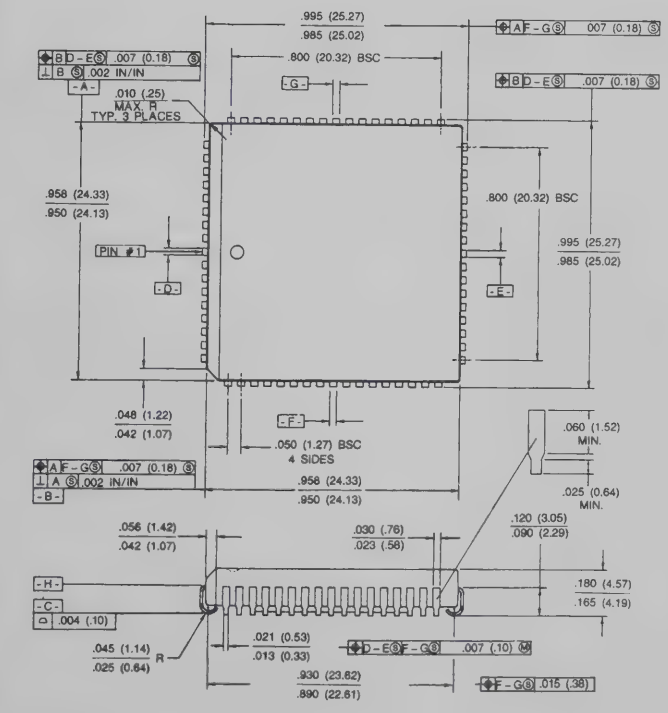
853-0397 081223

PO00642S

NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AD for plastic leaded chip carrier 52 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #52 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

PLCC-68



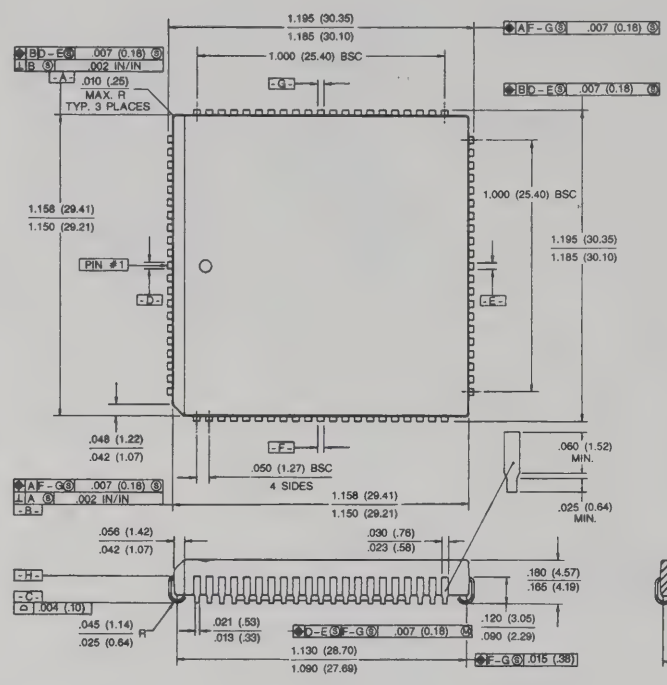
853-0398 081224

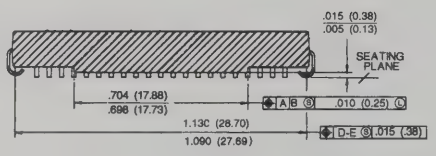
PO00622S

NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AE for plastic leaded chip carrier 68 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #68 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

PLCC-84





NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AF for plastic leaded chip carrier 84 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982.
4. "A" and "B" are reference datums on the molded body at plane "H" and do not include mold flash. Mold flash protrusion shall not exceed .006" (.15mm) on any side.
5. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
6. Pin numbers continue counterclockwise to pin #84 (top view).
7. Signetics order code for product packaged in a PLCC is the suffix A after the product number.

853-0399 081225

PO00592S

Adhesive Application and Curing

An Introduction

The use of adhesives in electronics isn't new. Epoxies and silicones, for example, have been used for encapsulating and potting components for years. But the application of an adhesive, either to component or substrate, as a means of holding the components in position prior to soldering, is new, and specific to surface mounted device (SMD) substrate assembly.

Unlike conventional through-hole (leaded) components which, once inserted into holes in a substrate, are held in place by clinching the leads, SMDs are simply placed onto the substrate surface with no inherent means of holding them in place (see Fig. 1). So in most cases, it's necessary to use an adhesive to form a bond until wave soldering can take place.

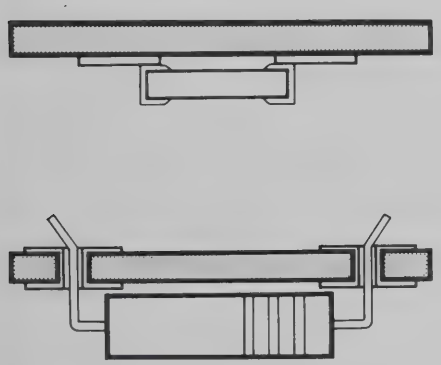


Fig. 1 SMD's, unlike through-hole components, have no convenient means of holding them in place prior to wave soldering.

Reflow-soldered SMD substrates (all soldering techniques are covered in detail in another publication in this series, titled SMD SOLDERING TECHNIQUES) are an exception to this as they use a solder paste applied to the substrate before the SMDs are placed. Here, the paste has sufficient adhesion to hold the SMDs in position until the solder is reflowed.

However, reflow soldering isn't suitable for all types of SMD assembly. For example, a Type II, mixed-print substrate (a combination of both SMD and through-hole components) must use the wave soldering technique, or combination wave/reflow soldering, so an adhesive is essential to hold the SMDs in place.

This adhesive must hold the device in the correct orientation upon placement, maintain it during the physical handling before final assembly, and withstand the adverse environments of fluxing plus the high temperatures of the solder wave.

After soldering, however, the adhesive's function is complete and it becomes a potential problem area. It may, for example, absorb moisture and become a conductive leakage path. Or it may degrade in an undesirable way. These considerations, plus methods of application and curing, govern the selection of an adhesive for SMD assembly.

Which Adhesive?

To determine which is the best adhesive for SMD assembly, an outline specification for an "ideal" adhesive is used to evaluate the various adhesive types. This specification gives the characteristics of the adhesive itself, plus factors relating to the application and curing processes, and environmental elements such as toxicity and flammability:

Physical Characteristics

- Stable one-part (single component) system
- Long shelf-life—without the need for refrigerated storage
- Good void filling—fills gap between substrate and SMD
- Thixotropic—good drop profile and no adhesive migration
- Electrically non-conductive—no possibility of short-circuits
- Non-corrosive—will not attack component or substrate
- Sufficient pre-cure tackiness—to pull SMD from pick-and-place unit
- Adequate post-cure bond strength—for reliable handling
- Chemically stable—will not react with flux and cleaning solvents
- Distinctive color—assists visual inspection

Process Considerations

- Application method—pin-transfer, pressure-syringe, or screen-printing
- Short cure time with low-energy cure—allows in-line curing
- Resistance to high temperatures—encountered during wave soldering
- Repair possibilities—removal of component after curing

Environmental Considerations

- Non-flammable
- Non-toxic
- Odorless
- Non-volatile

Of the many adhesives available, none fits all these requirements exactly. There are, however, many that can bond ceramic or plastic SMDs to

various substrate materials, each with its own advantages and disadvantages. Below is a brief description of four groups of adhesives, classified by chemical composition.

Thermosetting adhesives—cured by chemical reaction to form a cross-linked polymer. The thermosets are strong, structural adhesives, and once cured, by heat or catalytic action, cannot be softened to establish new adhesive bonds. Examples—Epoxy, acrylic, phenolic, polyester.

Thermoplastic adhesives—the thermoplastics do not change chemically when establishing a bond, and can be re-softened any number of times to form new adhesive bonds. Typically used in lightly stressed, non-structural, applications.
Examples—nylon, EVA copolymer.

Elastomeric adhesives—a subset of thermoplastics, these adhesives have great elasticity, and are formulated from synthetic or naturally occuring polymers in solvents, latex cements, or dispersions. Particularly noted for their flexibility.
Examples—rubber, silicone, neoprene.

Toughened alloy adhesives—formulated by blending rubbers and resins, both natural and synthetic, these adhesives are a special type of thermosetting adhesives. Developed for specific functions, these adhesives combine high strength with resistance to shock-loading.
Examples—epoxy-nylon, phenolic-neoprene.

Some of these adhesives have a proven track-record in the electronics industry. For example, the thermoset epoxies are probably the oldest and most-used engineering adhesives, and are available as one-part or two-part systems in the form of liquids, pastes, films, and powders. Cured by chemical reaction through heat, the **epoxies are best suited to automated SMD placement processes.**

Another popular group of adhesives, the cyanoacrylates, are not true one-part systems, but "one-part application" adhesives. This means that although they require two parts, only one need be applied as the second is supplied by the surfaces to be bonded in the form of absorbed moisture. Consequently, the polymerization is a surface initiated process, and cyanoacrylates function best with close fitting parts. This limits their application possibilities for SMD assembly, particularly when using MELF components (for example, leadless diodes with an SOD-80 encapsulation) which cannot use cyanoacrylates.

The alloys and elastomers, due to their specialized nature, are not generally used for SMD assembly, although an acrylic-rubber combination had been formulated as a pressure-sensitive adhesive for use with SMDs.

Other adhesives to be considered for SMD applications are the acrylics and the anaerobics. Although they don't have an extensive history of use in the electronics industry, they do have certain characteristics that are suitable for use in SMD applications. Table 1 lists the advantages and disadvantages of these four types of adhesive in SMD assembly.

Comparing the characteristics of the adhesives given in Table 1 with those for the "ideal" adhesive for SMD assembly illustrates that some trade-off has to be made. In many cases, the choice of adhesive limits the choice of application method. For example, the cyanoacrylates may only be applied by syringe.

Ultimately, the user should first determine the application process best suited to the type of substrate to be loaded, then choose a machine capable of this process (either a stand-alone adhesive application station or

Table 1. Advantages And Disadvantages Of Various Adhesive Types

Adhesive	Advantages	Disadvantages
Epoxy (one and two part systems)	• Proven history in electronics • High temperature use • Excellent solvent resistance • Excellent moisture resistance • Good void filling characteristics • UV cure systems available	• Limited shelf life • Longer cure time (one-part) • Higher cure temperature (one-part) • Complex application system (two-part) • Single application method (two-part) • Refrigerated storage (one-part)
Cyano-acrylate	• Very fast bonding • One-part system • Long shelf-life • Room temperature storage	• Single application method • Hazardous application • Bad void filling • Fair moisture resistance
Acrylic	• Moderate cure time • Good moisture resistance • Good solvent resistance	• Complex application system
Anaerobic	• One-part system • Unlimited shelf-life • Simple, inexpensive cure • High temperature resistance • UV cure systems available • Room temperature storage • Good solvent resistance	• Incompleteness of cure • Chemical activity • Low bond strength

one integrated into a pick-and-place machine), and finally, select the ideal adhesive for the machine. Such an adhesive will quite often be the responsibility of the machine manufacture, as they will have designed the machine with a specific adhesive type in mind.

So the selection process is:

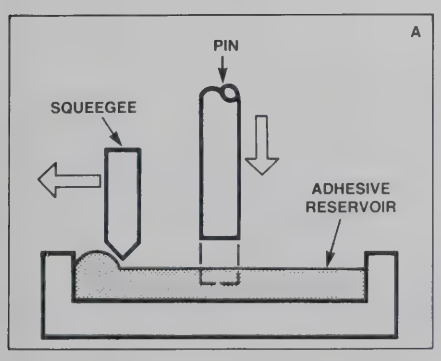
1. PROCESS
2. MACHINE
3. ADHESIVE

Experience has shown that a thermoset epoxy adhesive is best suited to pin-transfer application on pick-and-place machines. It has excellent precured properties (simple, trouble-free dispensing, good fill characteristics and good dot formation); effective curing chemistry (no undesirable gas release or adhesive migration); and ideal post-cured properties (resistance to damage during handling and to the high temperature of the soldering operation). It also has shown no long term influence on device or substrate.

Adhesive Application

There are three methods to be considered for automatically applying adhesives in surface mounted device assembly. They are:

Pin-transfer—in which a pin picks up a droplet of adhesive from a reservoir and transfers it to the surface of the substrate or component; surface tension causes a portion of the droplet on the pin to form a dot on the substrate (or component). See Fig. 2.



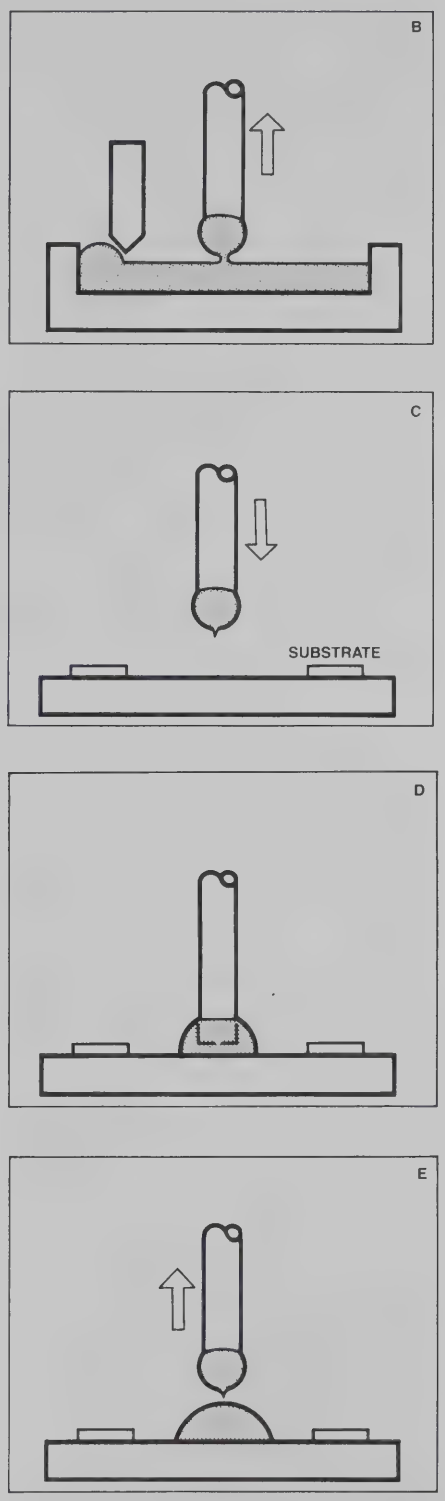


Fig. 2 Pin-transfer adhesive application.

Screen-printing—in which a fine mesh screen, coated except for the areas where adhesive is required, is placed over the substrate. A squeegee passes across the screen and forces the adhesive through the uncoated areas of the mesh and onto the substrate. See Fig. 3.

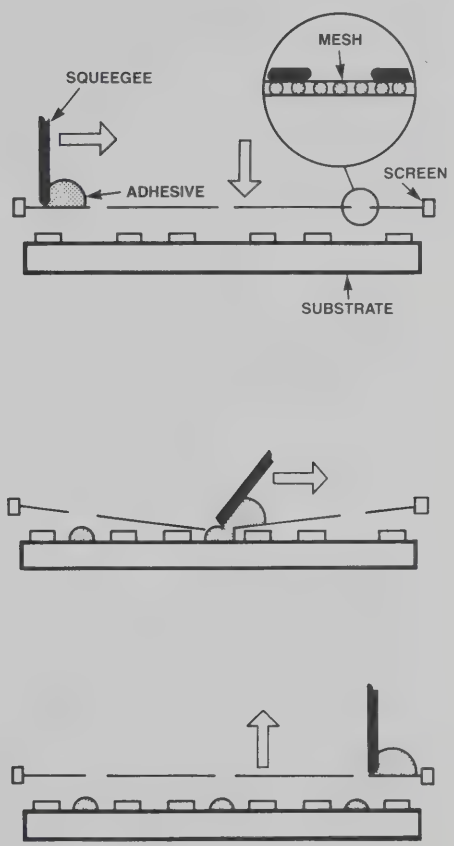


Fig. 3 Screen-printing adhesive application.

Pressure-syringe—a software-controlled syringe dispenses the adhesive from an enclosed reservoir by applying air pressure for a fixed time. The adhesive dot size is determined by the size of the syringe nozzle, and by the duration and magnitude of the applied pressure. See Fig. 4.

Manual application of adhesive can only be considered for prototyping, development work or repair, with an operator using a hand-held dispenser.

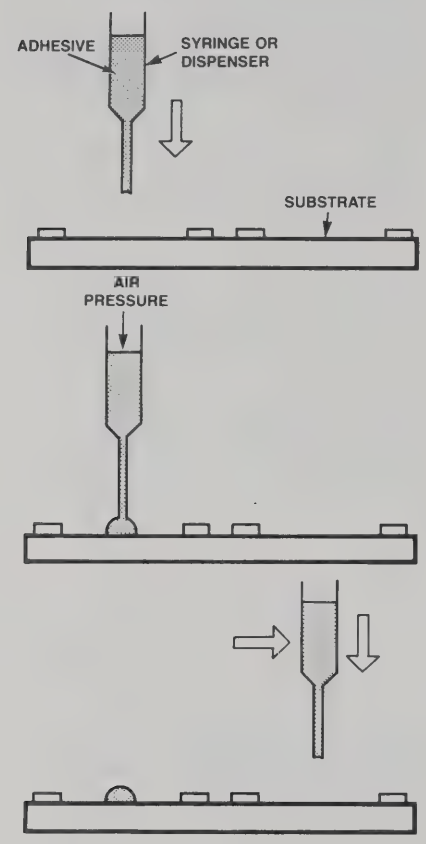


Fig. 4 Pressure-syringe adhesive application.

The advantages and disadvantages of each automated system are summarized in Table 2.

Table 2. Adhesive Application Methods - Advantages And Disadvantages

Method	Advantages	Disadvantages
Pin-transfer	• Compact system • Simple process • Little maintenance required • Simultaneous dot placement • Easy cleaning • Control of adhesive quantity	• Flat surface only • Dependent on adhesive uniformity • Open System
Screen-printing	• Simultaneous dot placement • Simple process • Easy cleaning • Uniform dot size	• Flat surface only–with no obstructions • Screen maintenance required • Open system
Pressure-syringe	• Accomodates irregular surfaces • Control of adhesive quantity • Uniformity • Closed system • Handles most adhesives	• Lot of maintenance required • Large size of system • Difficult cleaning • Fewer dots simultaneously

Pin-Transfer

Pin-transfer is the simplest mass application method for automated high-volume production machines. With this method you can either apply the adhesive to the substrate, or directly onto the component.

Application of adhesive to the substate requires a fabricated pin-array that exactly corresponds to the adhesive positions on the substrate (See Fig. 5), and the adhesive application stage must be incorporated in the substrate assembly line immediately before the SMD's are placed. Curing of the adhesive must take place shortly after SMD placement. The pin diameter and shape, the depth to which the pin is dipped into the reservoir and the viscosity of the adhesive determines the dot size.

During the transfer of the adhesive dot from pin to substrate, the pin must not touch the substrate surface as this will distort the resulting dot profile. Therefore, the substrate must be relatively flat and free from distortion. However, to ensure that the pin doesn't distort the adhesive dot, the tip of the pin is modified as shown in Fig. 6. This smaller diameter pin tip prevents the main bulk of the pin touching the substrate, but is of too small a diameter to have any significant effect on the resulting dot profile.

The nature of the pin-array makes it possible to apply the adhesive to a substrate that has already been loaded with through-hole (leaded)

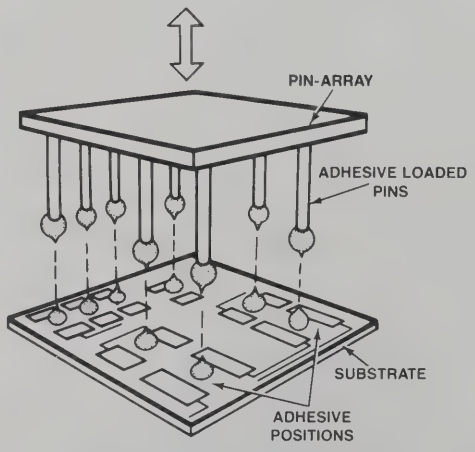


Fig. 5 Pin-transfer by pin-array directly onto the substrate.

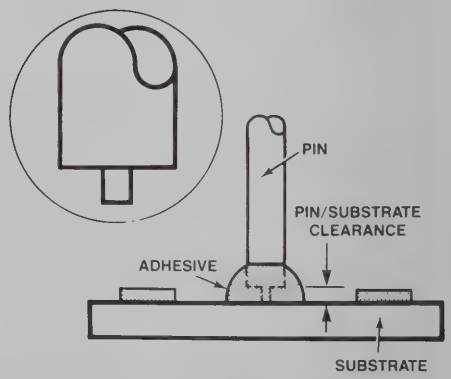


Fig. 6 The pin mustn't touch the substrate surface.

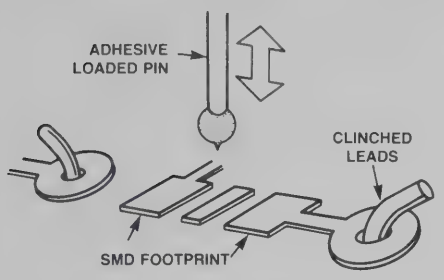


Fig. 7 The pin can apply adhesive between the clinched leads of through-hole components.

components on the other side (a mixed-print substrate) since the pins fit between the clinched leads of components as shown in Fig. 7.

Once placed, the adhesive dot must accept the SMD from the pick-and-place unit, and these may be of two types: a vacuum pipette that holds the SMD by vacuum alone; or a jawed chuck that holds the SMD incorporating a vacuum pipette to sense the presence of a component. For this latter system, the adhesive must have sufficient uncured tackiness to pull the SMD from the vacuum sensing pipette.

The alternative pin-transfer technique, where adhesive is applied directly to the SMD, is show in Fig. 8. Here, the pins apply the adhesive to the component from below, immediately after they have been taken from the tape

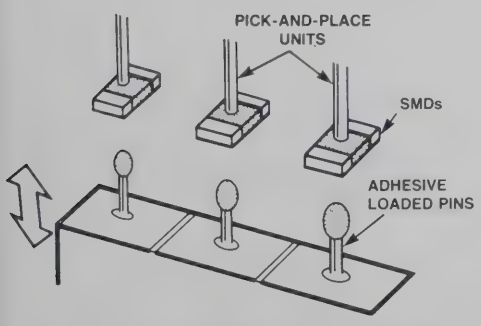


Fig. 8 Pin-transfer of adhesive directly to the SMDs.

reels by the pick-and-place units. This system had the advantage of not requiring a purpose-made pin-array and is therefore suited to smaller production runs where several slightly different versions of a design may be required. The tooling costs are lower as the number of pins employed by the machine is software programmable.

Screen-Printing

Like pin-transfer, the screen-printing technique places all adhesive dots simultaneously. Also like pin-transfer, it requires the substrate to be flat and distortion-free, but unlike pin-transfer, there can be no protrusions or obstructions on the surface as this will prevent the screen making contact with the substrate. Therefore, screen printing cannot be used for adhesive application of pre-loaded mixed-print substrates.

The adhesive dot size is determined by the size of the exposed area in the coating on the screen-mesh, the thickness of this coating (shown in Fig. 9), the mesh density, and the viscosity of the adhesive. Although essentially a very simple application method, screen-printing does have certain drawbacks regarding the high level of maintenance required. For example, the screen must be kept scrupulously clean as a blocked mesh inhibits dot formation.

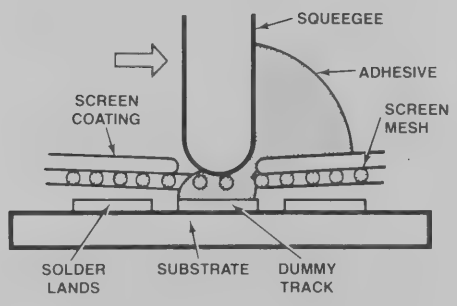


Fig. 9 Section showing the principle of screen-printing adhesive.

A similar method of adhesive application is that of stencilling. Here, a rigid stencil without a mesh is used in place of the screen, and the adhesive is sprayed through the apertures onto the substrate.

Pressure Syringe

The main advantage of the pressure-syringe method is that it allows different amounts of adhesive to be applied to different positions. Moreover, by using an adhesive with a specific rheological (flow) characteristic, relatively high dots can be realized as shown in Fig. 10.

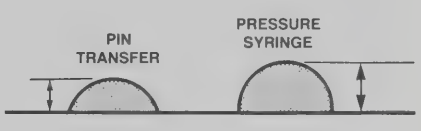


Fig. 10 Dot height is determined by adhesive type and application method.

This method, however, is difficult and slower than the others as fewer dots can be placed simultaneously, thus limiting its high-volume production potential. But for smaller production runs, and substrates with fewer SMDs, the flexibilty provided by the software progammability of this system is certainly advantageous.

Adhesive Dot Height Criteria

The amount of adhesive applied to each position is critical for two reasons: first, the adhesive dot must be high enough to reach the SMD, and second, there mustn't be too much adhesive which may foul the solder land and prevent the formation of a good solder joint.

The two dimensions (substrate metallization height, A, and SMD metallization height, B) that determine the minimum height of the adhesive dot (C) are shown in Fig. 11. This diagram illustrates that C must be greater than (A + B) for the dot to reach the

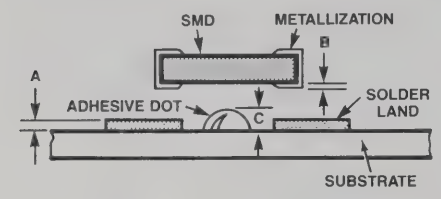


Fig. 11 Adhesive dot-height criteria.

SMD when placed. **In practice, C should be at least twice (A + B) for the formation of a good, strong bond.**

Taking these parameters in turn, the substrate metallization height (A), can range from about 35 μm for a normal print-and etch PCB, to 135 μm for a plated-through-hole board (see Fig. 12). And the component metallization height (B), for example of R/C1206 passive devices, varies between 10 and 50 μm.

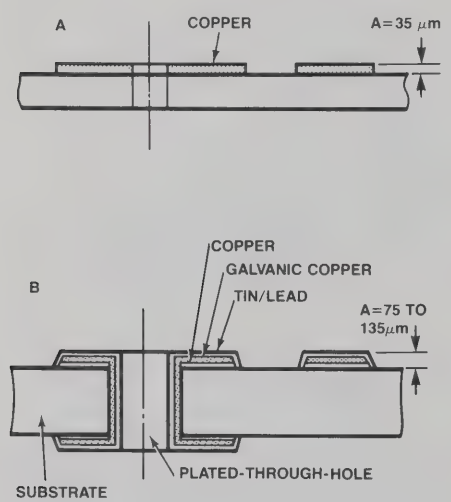


Fig. 12 Variation in substrate metallization height.

The variation in the lead standoff height (corresponding to dimension B) for SOT-23 and SOT-143 devices or SO ICs is even greater. The standoff distance (B) is 178 ± 76 μm for the SO and 203 ± 101 μm for the SOL.

These packages were primarily intended for reflow soldered substrates since a standoff distance much greater than 100 μm is not advisable for use with adhesives. Clearly, this poses a problem for the dot height criteria, for (A + B) can vary considerably on any one substrate. But, as it's advantageous to apply the same amount of adhesive to all placement positions, some compromise is necessary.

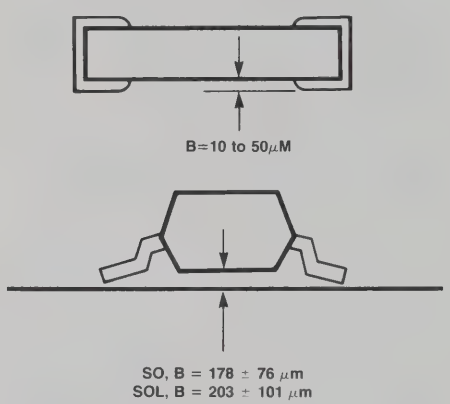


Fig. 13 Variation in SMD metallization height/lead standoff height for: R/C1206 (top), and SOT-23 or SOT-143 (bottom).

Dummy-Tracks

A solution to this problem is to put a track under the device, as shown in Fig. 14. This will help eliminate the substrate metallization height (A), from the adhesive dot-height criteria (although, it must be borne in mind that a track 0.3–0.5 mm [.012–.020″] will not completely support a drop with a diameter of 1.0–1.2 mm [.040–.048″]). Consequently, (C) can be a virtual constant. Quite often, the high component density of SMD substrates makes it essential to route tracks between solder lands and where it doesn't, a short dummy-track should be introduced.

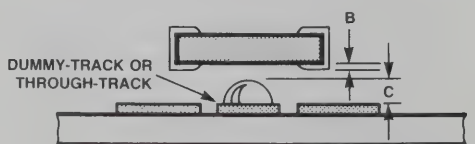


Fig. 14 Modifying adhesive dot-height criteria with a dummy-track.

In practice, it's possible to run two tracks under the R/C12106 size case and most other SMDs, and these are often covered with a solder-resist, as shown in Fig. 15. The resist further reduces the amount of adhesive required and the double tracks provide a broader base on which the dot can be applied.

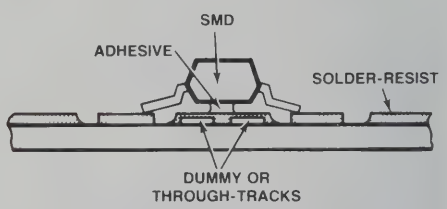


Fig. 15 Double tracks with solder resist.

One dot of adhesive is sufficient for bonding discrete SMDs and small-outline transistors and diodes, and for SO ICs up to 16 pins. The larger SO IC packages require two dots of adhesive, so the through-tracks (or dummy-tracks) must be positioned beneath the IC accordingly.

Solder Land Contamination

Contamination of the solder land with even a very thin layer of adhesive has very serious consequences for the soldering process. Many commercial adhesives are transparent when spead into thin layers, and if such a layer spreads onto the solder land, the solder will not form a good joint. For this reason, the adhesive viscosity must be correct to prevent "bleeding", and the adhesive placement must be very accurate.

MELF Component Placement

MELF component (cylindrical SMDs, for example the SOD-80 diode encapsulation, see Fig. 16) placement can

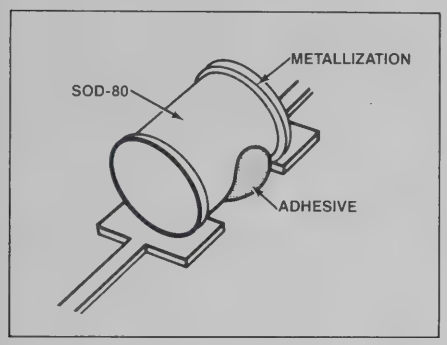


Fig. 16 Typical MELF component—the SOD-80 package.

present a problem if the component body does not hit the adhesive dot right in the middle. For when a cylindrical body is brought into contact with the hemispherical adhesive dot, the area of contact is very small indeed. Any deviation to either side of the center of the dot and the integrity of the adhesive bond may be seriously affected.

Take for example, the SOD-80 package. Along the center of this type of MELF, the lead stand-off height (dimension B in the dot height criteria) is about 0.1 mm. (.040″). A deviation of 0.5 mm. (.020″) either side of center results in dimension (B) increasing to nearly 0.4mm (.016″) unacceptable for the formation of a good bond.

Another problem with MELF components can arise if a substrate loaded with them is stored in a non-horizontal position (in an inclined rack, for example) prior to curing the adhesive. Due to the smaller adhesive contact area and the cylindrical shape, MELFs have a tendency to break free and roll down the substrate. Therefore, MELF loaded subrates should be kept in the horizontal position until the adhesive is fully cured.

Adhesive Curing

The method of curing an adhesive depends largely on the type of adhesive used. For automated placement machine applications, adhesives will generally use one or more of the following methods:

- Heat/Time—conventional oven or infra-red radiation
- Catalytic action—mixing with a hardener
- Ultra-violet (UV) radiation
- Anaerobic—the absence of oxygen

Curing By Heat/Time Plus Catalyst

Two-part epoxy systems consist of a resin and a hardener. When both constituents are mixed together, curing will proceed at room temperature, or be accelerated at elevated temperatures. The two parts can be combined by pre-mixing, or mixing at the application site, this latter method requiring a complicated metering and delivery system as accurate mixing in the correct proportions is necessary for rapid and complete polymerization.

A pre-mixed two-part epoxy has the hardener in suspension within the resin, only to be released when subjected to elevated temperature. This simplifies metering and application but limits the shelf-life.

A one-part epoxy has a limited shelf life but also requires refrigerated storage. In general, polymerization of one-part systems require moderately high temperatures for extended periods (although the actual requirements depend on the chemistry of the epoxy). A typical curing characteristic of a two-part thermoset epoxy is shown in Fig. 17 (warm-up time is excluded from the time axis).

The heat for curing is provided by a conventional batch oven or a infra-red radiation, and be either an on-line or an off-line (remote) process. Off-line curing places greater demands on the adhesive, since in the uncured state, it must have sufficient adhesion to withstand the mechanical handling involved in transferring substrates from the placement station to the curing station.

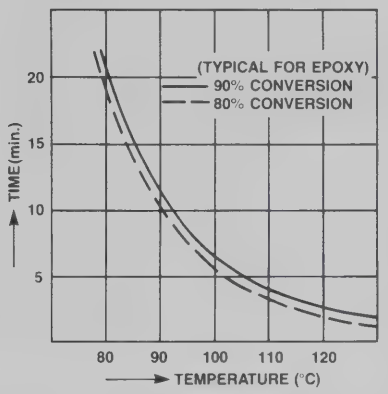


Fig. 17 Typical curing characteristic of a thermoset epoxy adhesive.

The manufacturing process also places certain demands on the adhesive. The two main processes for mixed print substrates are outlined in the flow charts of Figures 18 and 19. For the first process (through-hole components inserted before SMDs), the cured adhesive requirements are some minimal bonding and resistance to the solder wave. For the second process (SMDs placed before through-hole components), the demands on the cured adhesive are greater; it must now also withstand the mechanical shock, brushing and flexing incurred during the through-hole insertion process.

The maximum cure temperature is also influenced by these production techniques. For example, in the mixed-print design where the through-hole components are inserted before SMD placement and adhesive curing, the maximum cure temperature is determined by what the components (both SMD and through-hole) can withstand. If, however, the SMDs are placed and the adhesive cured before the through-hole components go in, it's only the SMDs and substrate material limitations that will influence the maximum cure temperature. The user must always check the components' specifications before subjecting them to elevated cure temperatures.

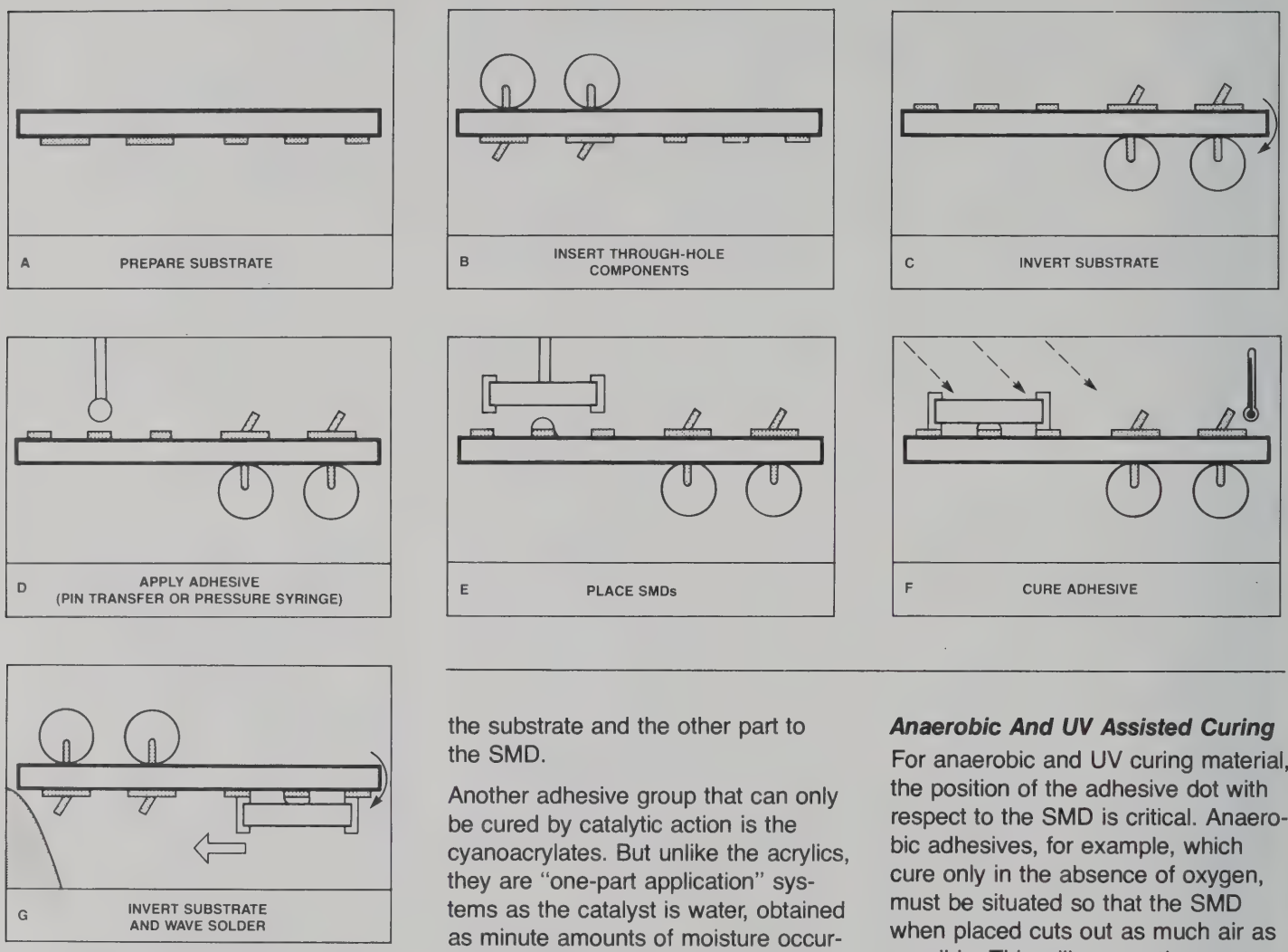

A PREPARE SUBSTRATE
B INSERT THROUGH-HOLE COMPONENTS
C INVERT SUBSTRATE
D APPLY ADHESIVE (PIN TRANSFER OR PRESSURE SYRINGE)
E PLACE SMDs
F CURE ADHESIVE
G INVERT SUBSTRATE AND WAVE SOLDER

Fig. 18 SMD mixed print substrate loading: through-hole components inserted first.

Curing By Catalytic Action Alone

Reactive acrylics are two-part systems (adhesive plus catalyst) that cannot be cured by any means other than the mixing of the two parts. When the two parts are mixed, polymerization starts and proceeds very rapidly. Consequently, they cannot be pre-mixed; the adhesive must be applied to one surface, the catalyst to the mating surface and curing takes place on contact. This places considerable limitations on reactive acrylics for SMD assembly as it involves a complex application system—one part to the substrate and the other part to the SMD.

Another adhesive group that can only be cured by catalytic action is the cyanoacrylates. But unlike the acrylics, they are "one-part application" systems as the catalyst is water, obtained as minute amounts of moisture occurring naturally on the surfaces to be bonded. Strong handling bonds are formed in 5 to 10 seconds and full cure strength is achieved in less than one hour.

Due to this rapid curing, they can only be dispensed from a closed system (pressure-syringe). Another drawback for their use in SMD assembly is their bad fill characteristics (they function best with close fitting parts—any gap greater than 0.25 mm. (.010″) requires an additional primer). Additionally, because they are almost universal adhesives which will bond skin to skin, machine part to machine part (and any combination thereof), care is needed when working with them.

Anaerobic And UV Assisted Curing

For anaerobic and UV curing material, the position of the adhesive dot with respect to the SMD is critical. Anaerobic adhesives, for example, which cure only in the absence of oxygen, must be situated so that the SMD when placed cuts out as much air as possible. This will assure the most rapid and complete curing.

On the other hand, with adhesives that cure by exposure to UV you must make sure that a portion of the adhesive is directly exposed to the UV source. This poses obvious problems with SMD assemblies, particularly with small-outline ICs, as the adhesive dot will be shielded from the UV by the component body. Polymerization may still occur, but at a much slower rate which means that curing may not be complete, and chemically-active material may remain under the device.

The alternative approach is to combine the properties of both groups and initiate the polymerization of anaerobic adhesives with long-wavelength UV radiation.

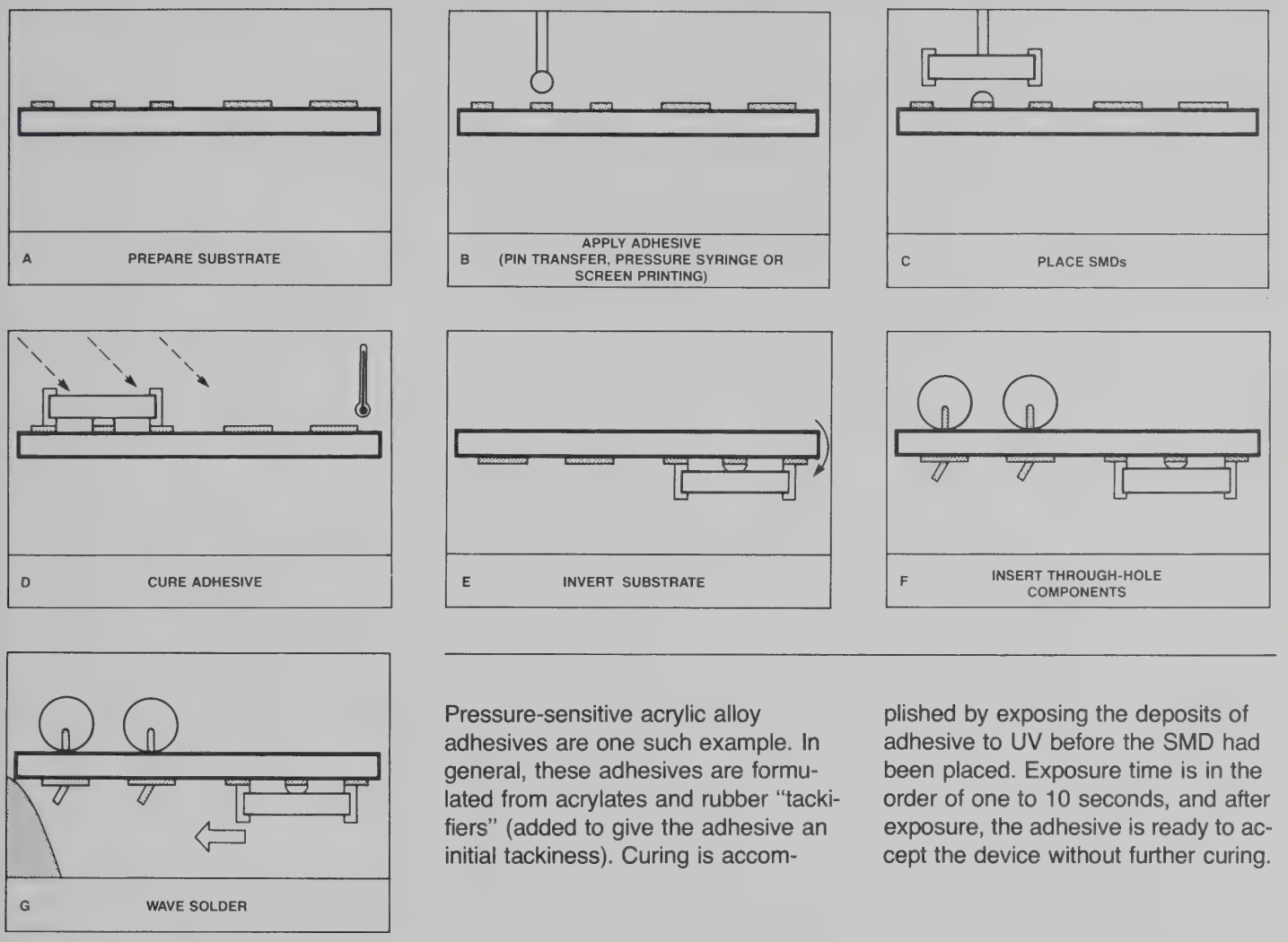

A PREPARE SUBSTRATE
B APPLY ADHESIVE (PIN TRANSFER, PRESSURE SYRINGE OR SCREEN PRINTING)
C PLACE SMDs
D CURE ADHESIVE
E INVERT SUBSTRATE
F INSERT THROUGH-HOLE COMPONENTS
G WAVE SOLDER

Fig. 19 SMD mixed print substrate loading: SMDs placed first.

Pressure-sensitive acrylic alloy adhesives are one such example. In general, these adhesives are formulated from acrylates and rubber "tackifiers" (added to give the adhesive an initial tackiness). Curing is accomplished by exposing the deposits of adhesive to UV before the SMD had been placed. Exposure time is in the order of one to 10 seconds, and after exposure, the adhesive is ready to accept the device without further curing.

Soldering Techniques

An Introduction

The SMD revolution in the electronics industry came in response to the need to pack more functional capability in a given enclosure, or the same capability into a smaller enclosure. And to do it with higher reliability and lower assembly costs. SMD technology can readily satisfy these needs in consumer, commercial, industrial, and military applications.

Despite all this, many manufacturers should anticipate problems during the transition to total or partial surface mounting. For them, it means a high capital outlay for production machinery, it will definitely mean an unfamiliar design and processing philosophy, and the possibility of mistakes during the learning phase. It is the aim of this publication to make this transition as painless as possible.

The spread of SMD technology beyond the realm of thick-film hybrids has prompted extensive research into machine-soldering techniques. The problems of flux corrosion, inspection, and testing, brought about by the high-density loading now possible with surface mounted devices is making zero-defect soldering the ultimate goal of all high-volume manufacturers.

This publication gives an appreciation of the possible pitfalls associated with the mass soldering of SMD populated substrates and an outline of the various soldering techniques currently available.

Soldering Techniques

For some time to come, the majority of manufacturers will use a mixture of surface mounted and through-hole components, and use wave soldering. However, with an ever increasing variety of components becoming available as SMD types, much of the research into soldering methods is being concentrated on reflow soldering.

Since no soldering technique yet exists which is universally applicable to all types of substrate containing SMDs, it is necessary to establish some form of unofficial classification. The various forms of populated substrates can logically be classified as follows:

Type I—Total surface mount (all-SMD); substrates with no through-hole components at all. SMDs of all types (SM integrated circuits, discrete semiconductors and passive devices) can be mounted either on one side, or both sides of the substrate. See Figure 1.

Type IIA—Double-sided mixed-print; substrates with both through-hole components and SMDs of all types on the top, and smaller SMDs (transistors and passives) on the bottom. See Figure 2.

Type IIB—Underside attachment mixed-print; the top of the substrate is dedicated exclusively to through-hole components, with smaller SMDs (transistor and passives) on the bottom. See Figure 3.

As a result of these manufacturing criteria, certain soldering techniques have become dominant. Modified wave-soldering is the most widely used method of soldering Type IIB circuits and reflow soldering is the predominant technique for Type I. Type IIA circuits are generally soldered using a sequential combination of these methods.

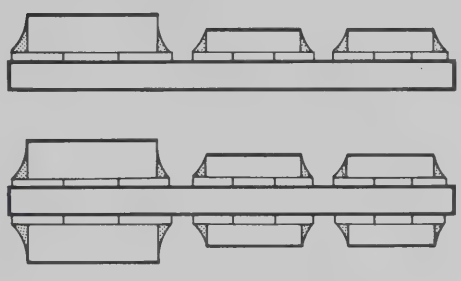


Fig. 1. Type I substrate—total surface mounting.

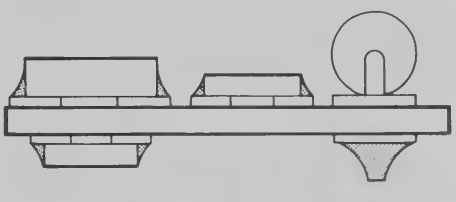


Fig. 2. Type IIA substrate—mixed print (double-sided).

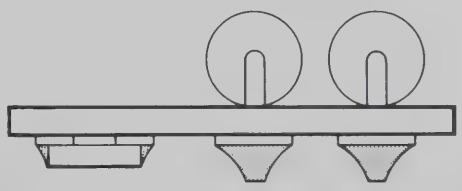


Fig. 3. Type IIB substrate—mixed print (underside attachment).

Type I

Maximum benefit from the use of SMDs is only possible by the complete elimination of all through-hole components. One or both sides of the substrate can then be populated with SMDs at very high density. With this high density, and if SO ICs and chip carriers are included among the components, reflow soldering is the only effective method of achieving high throughput levels.

As can be seen in Figure 4, the solder lands on the substrate are prepared, if necessary, and a combination of solder and flux in the form of a cream (or paste) is applied, either by screen or syringe dispensing. The components are then automatically placed. The solder cream is dried and the entire assembly is heated above the melting point of the solder to complete all joints simultaneously. This process is followed by cooling and the removal of flux residues, if required.

SMDs can also be attached to the underside of the substrate by the reflow method, either sequentially or simultaneously. Using the sequential method, side 1 is processed first, the substrate is then inverted and the process repeated. During the second reflow, the components on the underside are held in place by the surface tension forces in the molten solder joints.

Type IIA

The presence of through-hole components and SMDs on the same side of the substrate represents a mixed print circuit. It is envisaged that this type of circuit will be used extensively in the immediate future and for some time to come.

No single machine is yet available that can solder all levels of mixed print circuits; therefore, these substrates are currently produced in volume by sequential soldering employing both wave and reflow techniques, as shown in Figure 5. Here the solder paste is screened onto side 1 of the substrate, the SMDs are placed and the assembly is reflowed. Through-hole components are inserted, the substrate is then inverted and SMDs attached by adhesive to side 2. The assembly is then inverted again and wave soldered to complete the soldered joints. The SMDs on side 1 are not heated sufficiently by the solder wave to reflow the joints a second time.

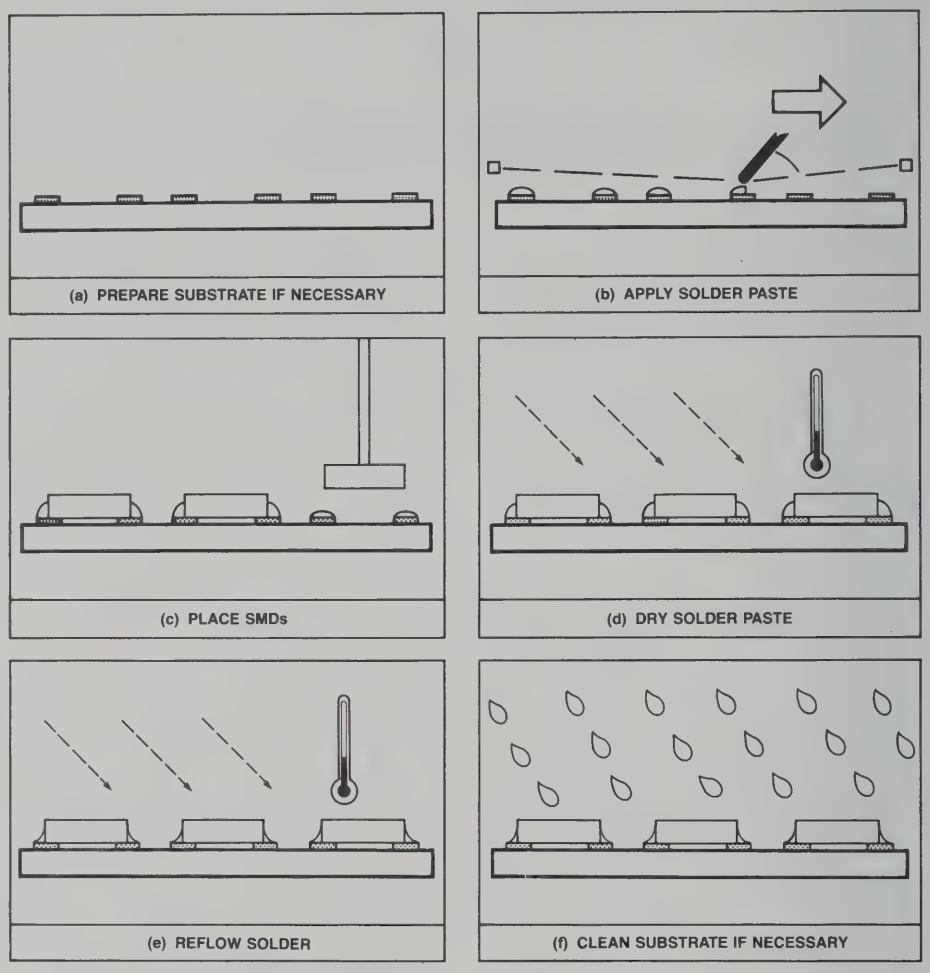

(a) PREPARE SUBSTRATE IF NECESSARY
(b) APPLY SOLDER PASTE
(c) PLACE SMDs
(d) DRY SOLDER PASTE
(e) REFLOW SOLDER
(f) CLEAN SUBSTRATE IF NECESSARY

Fig. 4. Reflow soldering of single- and double-sided total SMD (type I) substrates.

Type IIB

Leadless SMDs and SOTs are soldered to the underside of single sided, through-hole substrates exclusively by wave soldering as shown in Figure 6. Wave soldering has the advantage of being a well-established process in the electronic manufacturing industry and the modified versions of conventional wave soldering equipment, employing a dual wave, reduces the tendency to form solder bridges and un-wetted joints brought about by increased component density.

Wave Soldering

Conventional wave soldering equipment can be used for the soldering of surface mounted devices, but with increased circuit density and the resulting reduction of space between conductors, non-wetting and solder bridging can become a problem. These limitations are more acute with the larger active devices such as SO ICs. The closely spaced multiple leads on these components can cause bridging between adjacent leads on individual devices.

The dual wave method was developed to overcome these problems. The principle of the dual solder wave is that contact with the first wave, usually a turbulent wave with high vertical velocity, consumes or drives out most of the flux and ensures good solder

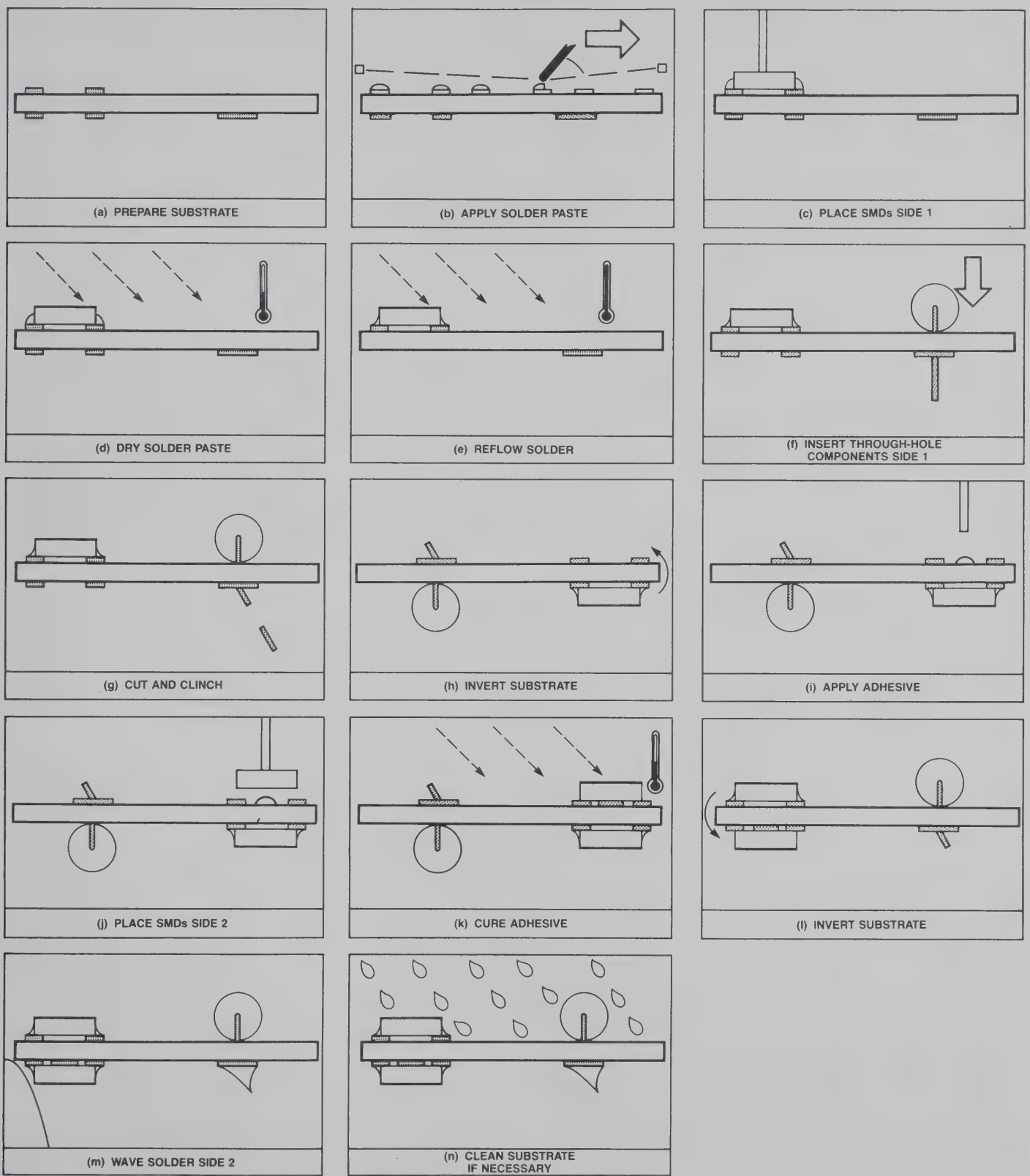

(a) PREPARE SUBSTRATE
(b) APPLY SOLDER PASTE
(c) PLACE SMDs SIDE 1
(d) DRY SOLDER PASTE
(e) REFLOW SOLDER
(f) INSERT THROUGH-HOLE COMPONENTS SIDE 1
(g) CUT AND CLINCH
(h) INVERT SUBSTRATE
(i) APPLY ADHESIVE
(j) PLACE SMDs SIDE 2
(k) CURE ADHESIVE
(l) INVERT SUBSTRATE
(m) WAVE SOLDER SIDE 2
(n) CLEAN SUBSTRATE IF NECESSARY

Fig. 5. Sequential reflow/wave soldering of mixed print (type IIA) substrates.

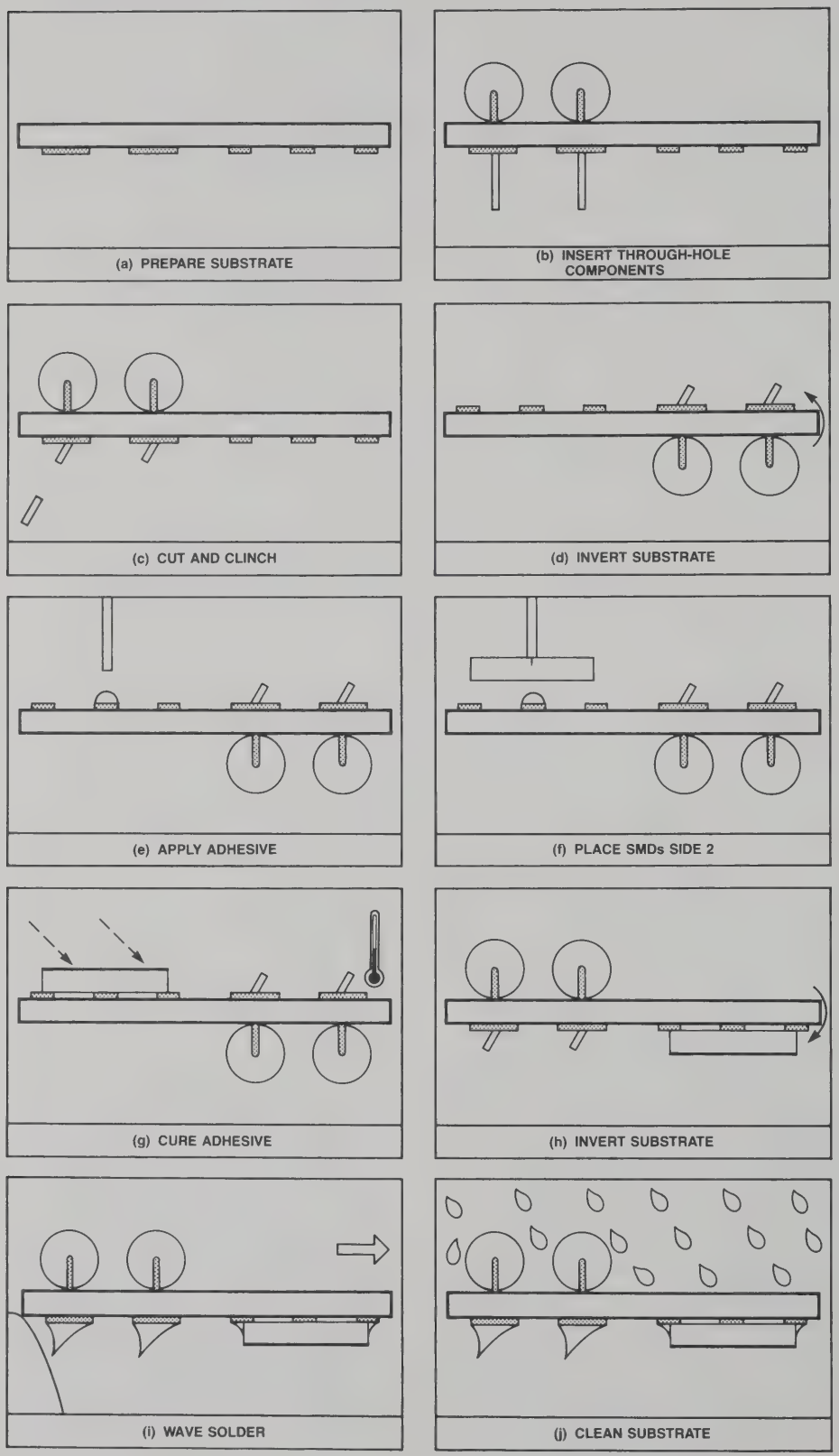


Fig. 6. Wave soldering of underside attachment mixed print (type IIB) substrates.

contact with both edges of the device. The second, laminar wave, then completes the formation of the solder fillet and removes bridges.

In a typical dual-wave soldering process, the preparation of the substrate is followed by the application of flux; usually based on a resin dissolved in an organic solvent such as isopropanol. This assures good wetting of the soldering surfaces.

Next, the board is preheated. This serves several purposes. First, it reduces the flux to the required viscosity, and second, it heats the substrate and components to a pre-determined temperature to reduce thermal shock and promote faster wetting. Preheating also minimizes the time spent at soldering temperature and so prevents dissolution of component metallization (leaching).

A variety of preheating systems are available, using forced hot air, quartz lamps or heated panels. During the preheat time, usually lasting about 10 seconds, the temperature of the substrate is raised to approximately 80°C. These values are approximate and will depend largely upon the composition of the substrate and the nature of the components.

After preheating, the underside of the substrate is brought into contact with the molten solder, first with the turbulent wave and then with the laminar wave. Experience has shown that a contact angle with the solder waves of approximately 7° gives optimum results. Figure 7(a) illustrates the dual-wave principle and Figure 7(b) shows an actual dual-wave machine. Figure 8 shows a theoretical time-temperature relationship for this process.

The introduction of oil onto the surface of the solder wave has proved beneficial when wave soldering densely populated SMD substrates. The lower surface tension provided by the oil reduces the tendency of the solder to form bridges as the substrate leaves the wave.

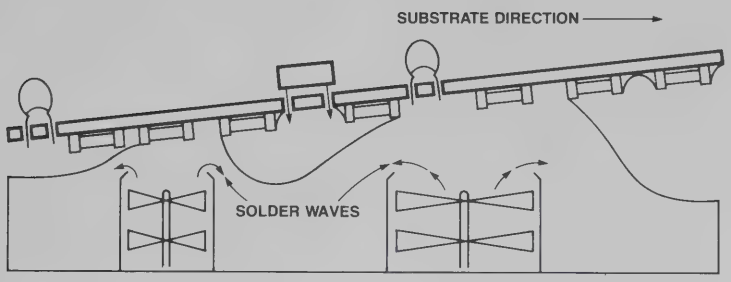


Fig. 7(a). The dual wave soldering principle.

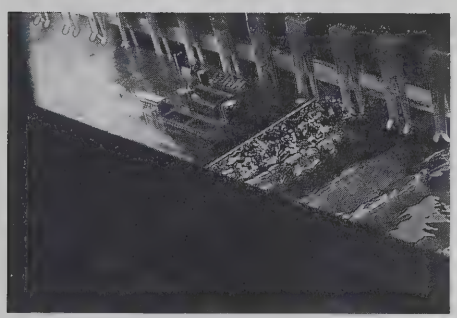


Fig. 7(b). A dual-wave soldering machine.

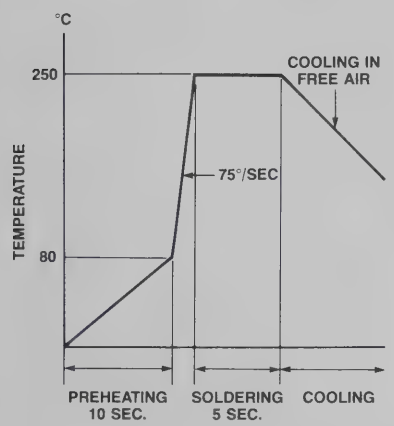


Fig. 8. The theoretical time/temperature relationship for wave soldering.

Some systems introduce a hot-air knife into the process immediately following the immersion stages. This directs a stream of hot air onto the underside of the substrate to remove excess solder thus eliminating solder bridges and icicles. This stage isn't required, however, if oil has been used.

Reflow Soldering

Solder cream reflow soldering has been used for hybrid assembly for some time and is potentially more versatile than the adhesive-attach/wave solder method.

A key ingredient in this process is the solder cream itself. It must be suitable for application by screen printing or dispensing, be resistant to solder balling, and it must reflow at the appropriate temperature. The flux residue must also be removable if necessary.

Solder creams consist of a paste flux impregnated with small nodules of solder. Solvents are added to the paste to produce optimum flow characteristics during screening. The shape of the solder particles is an important factor and normally spherical particles are recommended, although creams with non-spherical particles are also available and produce good results with very fine-line soldering.

Solder balling is a common characteristic of solder creams. This is isolated spheres of solder remaining on the substrate if the solder does not reflow correctly. These balls can result in reliability problems if not removed. Several factors can contribute to their formation.

If, for example, the cream is reflowed before the solvents have been completely evaporated they can boil-off and cause particles of solder to be ejected. Similarly, if the cream is overdried, solder balls may also be formed. It's therefore necessary to determine the optimum drying time and temperature for individual creams.

If the solder cream is poorly applied, and it extends beyond the periphery of the solder land, there is also more chance of solder balls occurring.

The purity of the solder is also of great importance. Creams with a high oxide content tend to produce more solder balls than those with low oxide levels. Tombstoning, or drawbridging may also cause problems. This phenomenon occurs when unequal wetting at either end of a passive component causes the component to up-end during the reflow process. The basic solderability of both substrate and component is therefore an important factor and is covered in another publication in this series titled *Component and Substrate Solderability.*

Solder Cream Application

Solder cream is applied to the substrate by one of two methods: screen printing or pressure syringe dispensing. Screening of the cream is the best high volume production method as solder is applied to all locations simultaneously. A stainless steel mesh, coated with emulsion except for the solder land pattern where cream is required, is placed over the substrate. A squeegee passes across the screen and forces solder cream through the uncoated areas of mesh and onto the lands.

The emulsion coating thickness, aperture size, mesh density and solder cream density determine the volume of cream deposited. Figure 9 shows a close up of the coated mesh showing the apertures corresponding to the solder lands, and Figure 10 shows the solder cream on the solder land prior to component placement.

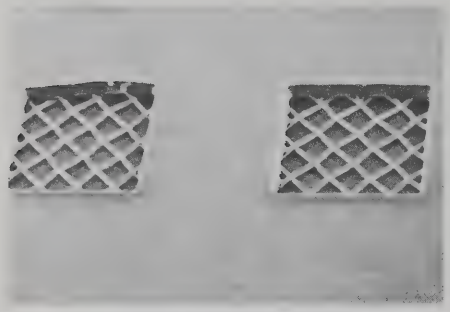


Fig. 9. The emulsion coated stainless steel screen for applying solder cream.

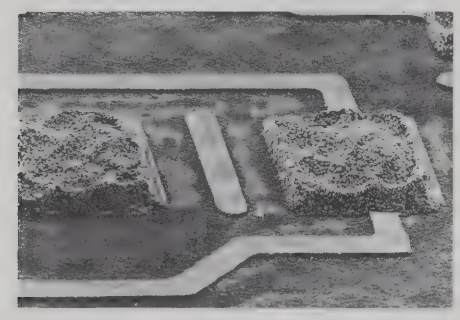


Fig. 10. Screen printed solder cream.

The dispensing method uses a syringe which sequentially applies a measured amount of solder cream to each location. Air pressure is used to dispense the cream, each application taking between 0.5 and 1 second. Although this method is comparatively slow, it is very flexible and useful in small production runs and in laboratory applications. Figure 11 shows a substrate with syringe dispensed solder cream prior to component placement, and Figure 12 shows the same substrate after reflowing.

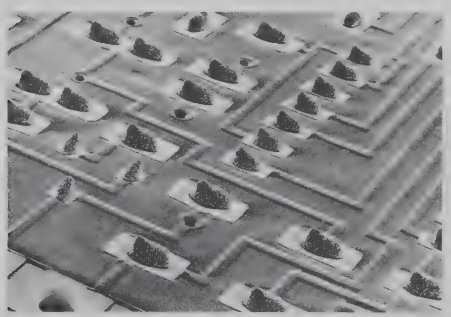


Fig. 11. Dispensed solder cream.

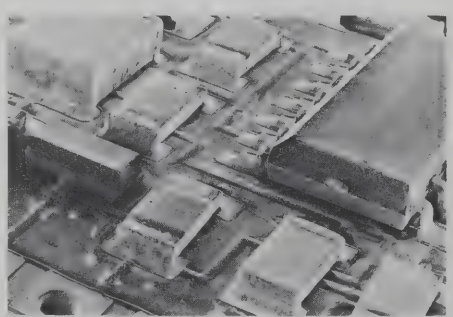


Fig. 12. The same substrate as in Fig. 11 after reflowing.

Reflow Techniques

There are several techniques available to provide the heat required to reflow the solder cream, all have advantages and disadvantages. The main systems used at the present time are thermal conduction, resistance soldering, infrared (IR) and vapor phase reflow.

Thermal conduction

Reflow soldering by thermal conduction is well known, owing to its extensive use in the hybrid circuit industry. In it, a conveyor belt carrying the populated substrate passes over two heater stages; a preheat zone to minimize thermal shock and drive off the flux solvents, and a reflow zone where the actual soldering is done.

Since it depends on intimate contact between the substrate and the heater plates, this method is only suited to small substrates with SMDs on the upperside only so that the substrate can lie flat on the conveyor. It is not suitable for larger substrates and those with components on both sides. Figure 13 shows a theoretical time/temperature relationship for thermal conduction reflow soldering.

Resistance soldering

Resistance soldering uses a heated element in physical contact with the joint to reflow the solder. It is mainly used for soldering quad-flat pack and very small outline (VSO) ICs with

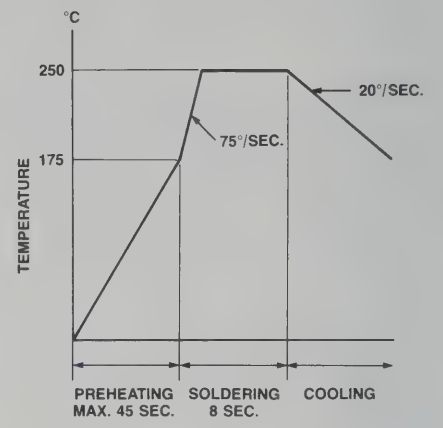


Fig. 13. The theoretical time/temperature relationship for reflow soldering.

long gull-wing type leads. This technique does not use solder cream, but an extra thick layer of tin/lead (approximately 20 μm) plated directly onto the solder land.

Each IC package type and size will require its own heating element, so this technique tends to be rather slow and restricted to development work on substrates with few ICs. It is also difficult to solder chip carriers and small leadless components. However, it is an excellent tool for de-soldering SMDs.

IR Reflow

Infrared reflow is another method used in the hybrid industry that can, with certain limitations, be used to reflow SMD populated substrates. Because it does not rely on heat conduction via the substrate it can be useful for the reflow of double-sided boards. Its main limitation is that the various materials used in the construction of the substrate and the component encapsulation absorb IR energy at different rates.

The metallization of chip capacitors and resistors is a good IR reflector, while the black epoxy used to encapsulate SO ICs and PLCCs is an excellent IR absorber. This results in an

uneven temperature profile across the board. However, these temperature differences can be reduced by extending the time under exposure to the IR source.

Vapor Phase Reflow

Vapor phase reflow soldering is done by heating a liquid fluorocarbon compound to its boiling point, (215°C in most cases) and immersing the substrate in the boiling vapors. The vapors condense and transfer heat to the board, using the latent heat of condensation principle. Since the liquid boils at a temperature higher than the melting point of the solder, the solder reflows. The temperature is accurately controlled by the boiling point of the liquid and heating is uniform over the whole substrate.

Simple vapor phase reflow has two drawbacks. The first is the high cost of the fluorocarbon compound, some of which is lost during the process. The second drawback is the environmental aspect. Some communities regulate the operation of systems that emit fluorocarbons, and others may do so in the future. The main concern being that if the liquid level in the system falls to the point where the heating coils are exposed, the compound can decompose and generate highly toxic fumes. A safety system must always be incorporated to ensure that this situation cannot arise.

Two recent developments have gone a long way to reduce costs by preventing vapor loss. One is the development of the dual-vapor system whereby a cover blanket of a secondary, less expensive and lighter vapor confines the more expensive primary vapor. This secondary blanket "floats" above the primary vapor.

The second development, a single-vapor continuous system, relies on mechanical means to prevent liquid loss.

Dual Vapor System

The dual-vapor batch soldering system consists of a tank containing the boiling liquid and two vapor zones as shown in Figure 14. An elevator tray, suspended from a hoist mechanism, conveys the substrate vertically in and out of the vapor zones. Primary and secondary condensing coils are located at appropriate levels around the inside of the tank to limit the upper level of each vapor zone by providing water-cooled surfaces upon which the excess vapors condense.

Initially, the bottom of the tank contains a mixture of both primary and secondary liquids. As the temperature is raised by the immersion heater, the secondary liquid starts to boil (at approximately 48°C), and the vapor rises in the tank. The upper level of the vapor is maintained, for a brief period, at the primary coils where the inlet water temperature is kept higher than the boiling point of the secondary liquid, usually around 55°C. During this period, the increasing temperature of the mixture causes the secondary liquid to superheat and it rises to the level of the secondary coils, maintained at between 7°C and 18°C.

Once the boiling point of the primary liquid has been reached (215°C), no further increase in temperature is possible. The rising primary vapor condenses on the primary coils, and falls back to the bottom of the tank, and so total evaporation is avoided.

As the secondary vapor is heavier than air and lighter than the primary vapor, it tends to remain in the tank, below the level of the secondary coils. The liquid produced by condensation on the coils is recovered and passed through a scrubber to remove acids. The scrubbed liquid, after the water has been extracted by a dryer, is returned to the tank.

The transfer of heat at the interface of the two vapor zones ensures that the secondary vapor is maintained in a superheated condition. This, together with the relatively high water temperature at the primary coils, prevents the secondary vapor condensing on them. Condensation of the secondary vapor, plus a very small amount of the primary vapor, occurs on the secondary coils. This small amount of primary liquid is not lost, but returned to the tank with the secondary liquid, via the acid scrubber.

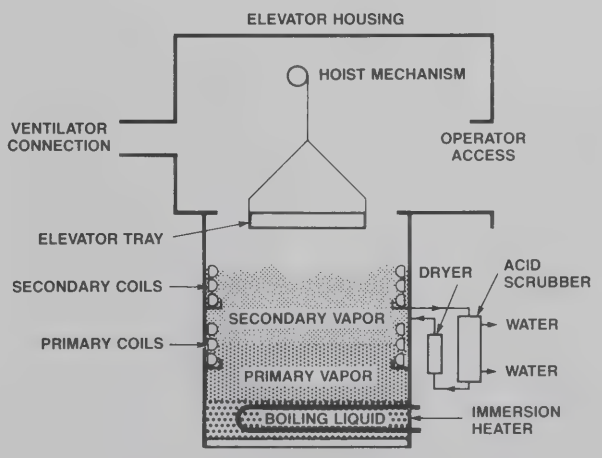


Fig. 14. Dual-vapor batch system schematic diagram.

The acid scrubber is a very important element in the system. Because the secondary vapor is superheated, it readily decomposes to form various gases, which, when combined with atmospheric water vapor, produce acids. These acids must be continually purged to prevent corrosion of the tank and unacceptable levels of ionic contamination on the substrates.

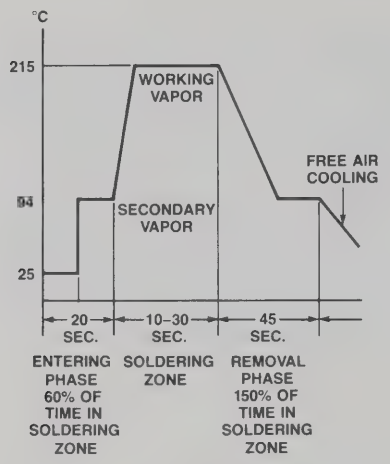


Fig. 15. The theoretical time/temperature relationship for dual-vapor reflow soldering.

Single-Vapor Continuous System

The major drawback of the dual-vapor system is the problem of secondary-vapor control. The correct maintenance of the secondary-vapor zone is essential in preventing loss of the primary vapor, thus holding operating costs to an acceptable level. As the secondary vapor is clear, and therefore difficult to see, visual monitoring is difficult.

The recognition of this problem has lead to the development of the conveyorized, single-vapor, in-line reflow system. As can be seen in Figure 16, vapor-loss control is achieved at the input and output throats of the conveyor thus eliminating the need for a secondary vapor.

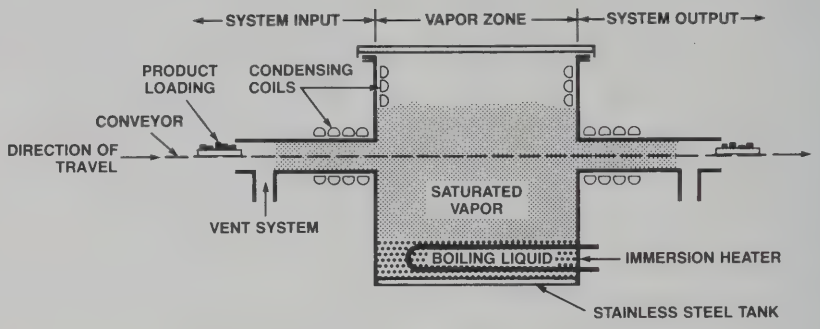


Fig. 16. Single-vapor continuous system schematic diagram.

The production of the primary vapor is similar to that for the dual vapor system, except that the zone limits are defined by the cooling surfaces at the conveyor throats, where migrating vapor is condensed and returned to the tank. As a result, vapor-loss control is no longer operator-dependent. Pre-heat, reflow heat and cooling are all interrelated by the machine geometry and consequently, conveyor speed is the only process variable.

The fully fluorinated organic compounds used to produce the primary vapor are available with boiling-points ranging from 56°C to 253°C, and the choice of compounds will be dictated by the composition of the solder paste being used.

The fluoro-carbon compounds are inert, and up to their boiling points, do not cause any chemical reaction with any of the materials normally used in electronic substrate processing. Consequently, in the processing area, containing a saturated vapor, no air or oxygen is present. Because of this inert environment, and the resulting freedom from oxidization, relatively small amounts of a very mildly activated rosin based flux are usually sufficient to produce high quality soldered joints.

Conclusions

Although wave soldering is a well-established process, it has some disadvantages in SMD application. Firstly, as the components are attached by adhesive to the substrate, prior to soldering, care must be taken that the adhesive does not contaminate the solder lands or component terminations, thereby affecting solderability and joint quality. Wave soldering also imposes design limitations, regarding component orientation and conductor spacing.

Reflow soldering also has drawbacks. The solder cream, for example, must be applied using either screens or dispensers. Another disadvantage is that some components, such as electrolytic capacitors, may not survive the longer periods at soldering temperatures, especially using vapor phase reflow.

Despite these limitations, vapor phase soldering is emerging as the candidate for a general reflow process as it is considered more acceptable than either IR or thermal conduction reflowing. Vapor phase is, however, more expensive to operate, and for this reason both IR and thermal conduction methods will probably continue to be used where circumstances permit.

Solder Joint Criteria

An Introduction

The decision to adopt SMD technology will be taken only after a thorough appraisal has been made of all the various assembly techniques available to the manufacturer. Techniques that enable the production of high-quality, reliable electronic assemblies by the most cost-effective means. Some are already in use for through-hole component substrate manufacture, but many are new, and specifically designed for SMD assembly.

Although the advent of high-speed, accurate SMD placement machines and improved mass-soldering methods has greatly reduced the human involvement in the assembly process, one area remains where skill, training and judgment are the most important factors: inspection of the solder joints.

The increasing component density and decreasing component size of SMD assemblies is stimulating research into solder-joint inspection methods for substrates either totally or partially populated with SMDs. Although systems are being developed that use pattern recognition to check a substrate for missing or misaligned components, visual examination by a trained inspector still remains the most practical method for verifying the quality and reliability of the soldered joint.

This publication describes and illustrates the criteria by which the trained inspector can assess the quality of the finished substrate and the reliability of the soldered joint.

Inspection

Several forms of inspection method are available, the naked eye, microscope, and video are examples. Of these, the most widely used is the eye, with or without the aid of a magnifier having 2× or 3× magnification and integral lighting. A magnifier is recommended for the smaller, more densely populated substrates, since, apart from making inspection easier, it also reduces operator fatigue.

Typically, a general inspection is first made of the soldered side of the substrate. Overall appearance should be pleasing to the eye, all joints having a similar appearance, the length of the through-hole component terminations should be within the prescribed limits and the substrate should be clean. This will be followed by an appraisal of the upper side to check for solder flow in plated-through holes, displaced or missing components and general cleanliness. Next, the soldered side should be re-examined in detail for such obvious defects as missing SMDs, solder bridges, and residues and the individual soldered joints assessed for quality and reliability.

Unlike leaded component joints, where the lead also provides added mechanical strength, the SMD must rely on the quality of the soldering for both electrical and mechanical integrity. It is therefore necessary for the inspector to be trained to be able to make a visual assessment with a view to long term reliability.

Defects can occur in either the substrate or the individual joint. Substrate, or circuit defects, such as misaligned components, bridges, and solder balls are inclined to be the more obvious ones. Joint defects, however, are much more a matter of judgment and interpretation of the visual aspects, such as the degree of wetting, volume of solder or the shape of the joint.

Defect Classification

Defective solder joints are classified under three headings, as follows:

Major defects—are likely to result in the failure of the circuit to perform its intended function. These must always be rectified. The application of Statistical Quality Control (SQC) to frequently recurring defects can be very helpful in identifying the cause and indicating the appropriate action.

Minor defects—are unlikely to result in circuit failure. They form departure from established standards that has little bearing on the effective use or operation of the unit. The need for rectification depends upon the level of reliability required. Minor defects occurring in circuits intended for use in life support systems, or in the aerospace industry would be rectified, while those destined for the consumer market may well be ignored.

Cosmetic defects—those that have no effect on the function or reliability of the circuit, and therefore need not be rectified. However, their presence should invite an investigation into their cause.

Soldering Defects

Substrate, or circuit related defects will generally fall into the following categories: solder bridges, solder icicles and solder residues. Another defect, specific to reflow soldering of leadless components, is that known as "drawbridging." In wave soldering, adhesive contamination of contact areas can also introduce defects.

Solder bridges

Bridges are unwanted solder connections between metal parts of the circuit and can occur between adjacent conductors or terminations. When such a bridge causes a short-circuit between points of differing potential, or when it completes an unwanted ground-loop, it becomes a major defect. When it connects points at the same potential, it may be regarded as cosmetic, provided of course, that it does not form a ground-loop. Figures 1 shows bridge between the leads on a Very Small Outline (VSO) IC package.

Fig. 1. Solder bridges between leads of a VSO-40 package.

Bridging between passive SMDs placed end to end and connected by a conductor (see Fig. 2) constitutes a minor defect. This is because, even though the two terminations are at the same potential, the extra solder in the bridge produces a degree of rigidity that may well be unacceptable. Solder bridges occur much more often with wave soldering than with reflow methods.

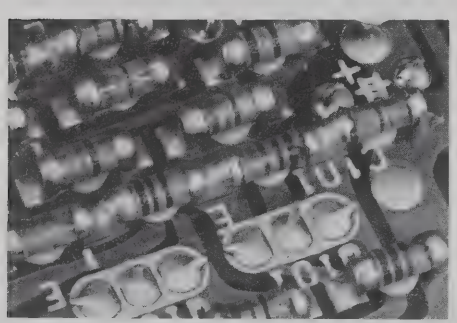


Fig. 2. Solder bridge between adjacent MELF resistors.

Possible causes of solder bridges:

Design Faults:

- Insufficient spacing of conductors, solder lands or components.
- Incorrect orientation of components.

Process faults:

- Excess solder; solder wave too high.
- Warped substrate resulting in flooding of substrate upper surface.
- Insufficient flux.
- Damage or misregistration of solder resist.
- Contamination of the solder bath.
- Insufficient oil intermix.

Solder icicles, or spikes

Apart from solder bridges, excess solder on the underside of the substrate can also result in the formation of icicles or spikes (see Fig. 3). These are formed when a filament of solder is drawn off the component terminations as the substrate breaks contact with the solder wave.

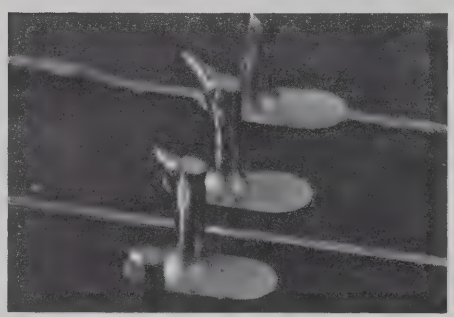


Fig. 3. Solder icicles.

Icicles are usually regarded as cosmetic defects, but when they significantly reduce the air insulation distance, especially on high-voltage circuits, they constitute a major defect. Like bridges, icicles are a product of wave soldering.

Possible causes of solder icicles:

- Contamination of the solder bath.
- Insufficient oil intermix.
- Uneven distribution of flux.

Solder residues

Solder residues can be identified as webs, skins, spatters or balls.

A web is a fine oxide thread, sometimes with solder particles attached, connected to the substrate or terminations. Being very thin, it is often difficult to see, particularly when occurring above the substrate surface. Webs can cause short-circuits and are always major defects (see Fig. 4).

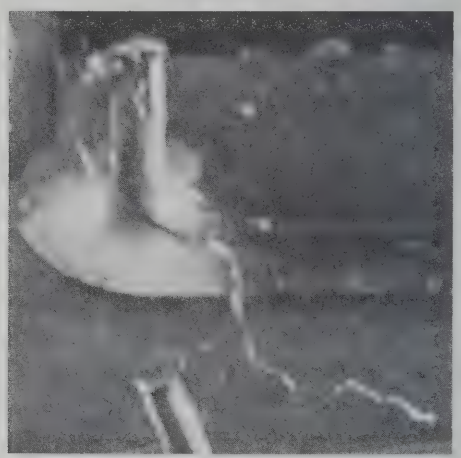


Fig. 4. Solder web.

A skin is a thin film of solder attached to the substrate and conductors. Like webs, skins can also cause short-circuits and are, therefore, major defects (see Fig. 5).

Fig. 5. Solder skin.

Solder spatters (or splashes) may be in the form of either small isolated solder skins attached to the substrate, or solder balls. Apart from causing short-circuits immediately after soldering, they can also cause failure in the

field if they become detached during use. Their classification as major or minor defects will depend largely on their size and location. Solder balling is shown in Fig. 6.

Fig. 6. Solder balls.

Webs, skins and spatters are usually the result of wave soldering. Solder balls occur with reflow soldering.

Possible causes of solder residues:

Wave soldering:

- Incorrect choice or application of flux.
- Solder contamination.
- Incorrect pre-heat time or temperature.

Reflow soldering:

- Incorrect pre-heat time or temperature.
- Incorrect choice of solder paste.

Drawbridging

Drawbridging is the standing up of leadless SMDs on one of their end faces (as shown in Fig. 7), particularly during vapor phase reflow soldering.

This phenomenon occurs when the solder cream reflows at one end of a leadless SMD before the other, and the forces exerted by the surface tension of the now molten solder "pulls" the SMD away from the still solid solder cream at the other end. These forces can be strong enough to up-end the SMD as shown in the illustration. Drawbridging is always regarded as a major defect.

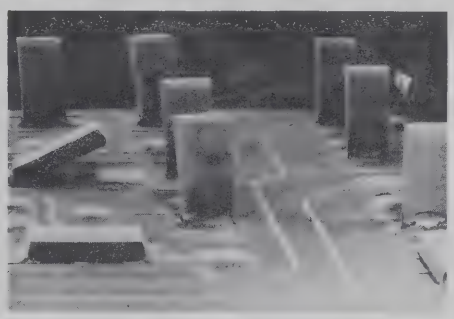


Fig. 7. The drawbridge effect.

Possible causes of drawbridging:

- Insufficient width of metallization under component.
- Wrong size of solder land.
- Incorrect measure of solder cream.
- Wrong type of solder cream.

Adhesive contamination

In wave soldering, the prior application of adhesive is a critical step (see *Adhesive Application And Curing*). As the tolerances are very tight, there is a great risk of the leads or solder lands becoming contaminated with adhesive. The result is that a joint will not be formed at all, or that only the extremity of the lead or metallization is soldered (see Fig. 8). This is a major defect.

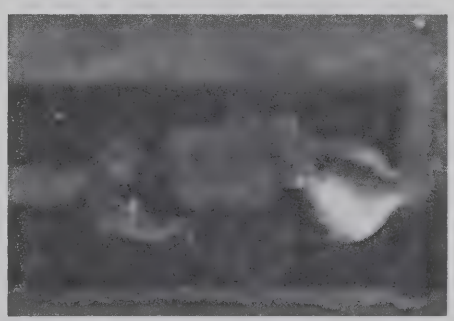


Fig. 8. Adhesive contamination.

Possible causes of adhesive contamination:

- Misplacing of adhesive on solder land or component.
- Adhesive with the wrong viscosity.
- Movement of SMD after placement on adhesive (particularly MELF).

Blow holes

During soldering, gas or flux can become entrapped in the solder and cause a void. These holes in solder joints vary in both size and type. As they are completely enclosed in solder, they cannot be detected visually, but they are usually present in most soldered joints. Figure 9 shows a cross-section through a soldered leadless SMD, revealing the holes on the solder meniscus.

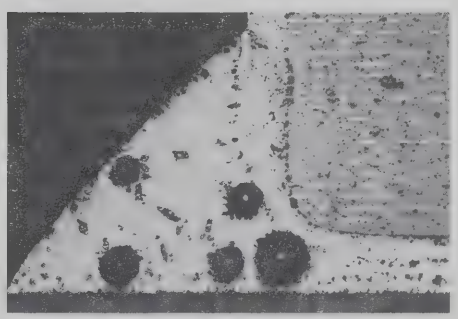


Fig. 9. Cross-section through a soldered leadless SMD revealing holes in the solder.

If, however, a void ruptures during solidification, then a blow hole results. Blow holes are irregular holes in the surface of the solder whose defect classification will depend on their size and location. True holes extend right through the joint and may well be large enough to significantly reduce the amount of solder in the joint, thus producing a major fault.

General Solder Joint Criteria

A good, reliable solder joint will perform both its electrical and mechanical function, without failure, during the lifetime of its associated assembly. In assessing the quality and reliability of the joint, irrespective of whether it is a through-hole component joint or an SMD joint, and irrespective of whether it was formed by wave or reflow methods, the inspector has three basic criteria upon which to base his judgment. These are:

- Good wetting of the surfaces.
- A sound and smooth joint surface.
- The correct amount of solder.

Good wetting

Good wetting is indicated by an even flow of solder over the surfaces of the solder land and component termination, and thinning toward the edges of the joint. A metallic interaction will have taken place, resulting in a smooth, unbroken and adherent layer of solder on the joint.

Non-wetting is a failure of the surface metal to be coated by molten solder, so that the original surface remains partially or totally visible. This may be due to contamination of the joint surfaces, insufficient fluxing, or too short a pre-heat time. Figure 10 shows non-wetting of a conventional through-hole solder joint.

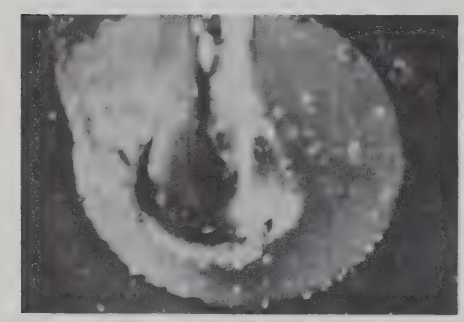


Fig. 10. A through-hole joint showing non-wetting.

If, after wave soldering, any joints exhibit total non-wetting, this may be due to a design shortcoming, whereby the joint has failed to come into contact with the molten solder due to the "shadow effect" (shielding of the joint by the component body or other adjacent components).

De-wetting on the other hand, is the withdrawal of molten solder from the surface after initial wetting. It is characterized by dispersed and irregular solder droplets on the joint surface, often with a thin film of solder between them. De-wetting becomes very evident at high soldering temperatures and long dwell-times. Figure 11 shows de-wetting of a conventional through-hole solder joint.

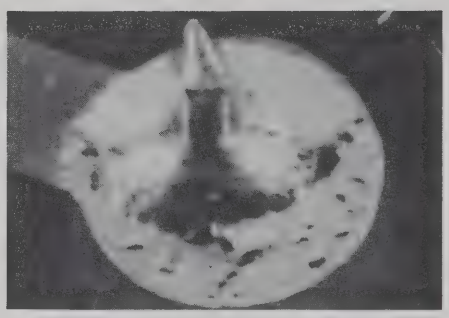


Fig. 11. A through-hole joint showing de-wetting.

This is usually indicative of contamination of the solder or joint surfaces, poor solderability or dissolution of the SMD metallization. Severe de-wetting often results in insufficient volume of solder at the joint. Various degrees of solder de-wetting on copper plates are shown in Fig. 12.

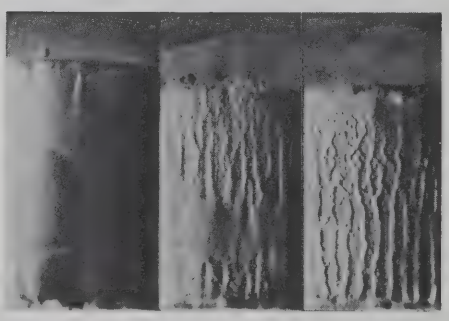


Fig. 12. Various degrees of wetting on copper plates, showing that as de-wetting increases, the solder forms irregular droplets.

Sound smooth surface

The surface of the solder should be smooth, shiny and uninterrupted. Eutectic tin/lead solder is uniformly shiny, except perhaps for the center of the shrinkage dimple sometimes present. However, the surface of 60/40 tin/lead alloy may have a rough surface after slow cooling. This is cosmetic and does not detract from the quality of the joint.

Correct amount of solder

A good solder joint should have neither too much nor too little solder. For mixed-print substrates with through-hole components, the shape of the leads should be recognizable within the contour of the joint. This applies particularly to clinched leads on the soldered side of a substrate without through-hole plating.

The solder should be seen to have penetrated completely through the plated holes in substrates loaded with components on both sides. In the case of single-sided substrates without plated holes, the solder should wet the entire solder land and should increase uniformly from the edge of the land up to the termination, forming a neat fillet.

SMD Joint Assessment

Although the criteria for the assessment of an SMD joint are basically the same as those for through-hole components, that is, good wetting, the right amount of solder, and a sound, smooth surface, there is an additional factor to be considered that is not applicable to leaded components. This is the misalignment of the component on the solder lands.

Some misalignment is usually inevitable, due to the tolerances on the component, the solder land, and the placement machine. Provided at least half the termination is within the boundaries of the solder land, then misalignment is acceptable (see Fig. 13). It may not, however, be cosmetically acceptable.

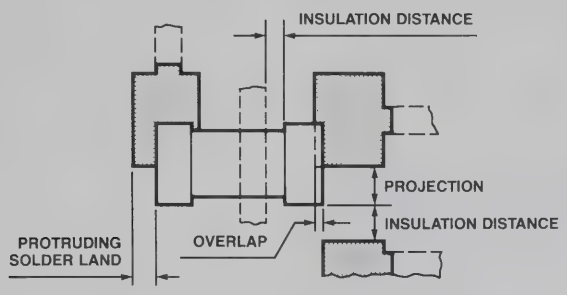


Fig. 13. Misalignment of leadless SMDs.

If the width of the solder land is greater than the width of the metallized connecting area of the component, then a projection smaller than half the width of the connecting area is a minor defect.

If, on the other hand, the width of the solder land is smaller that the width of the metallized connecting area of the component, then a projection is unavoidable. This is acceptable provided that the width of the solder land is completely covered. If the width of the solder land is not covered completely, but the projection is still smaller than one half of the width of the connecting area, the defect is a minor one.

When the degree of misalignment extends beyond these limitations, the fault is major one. The resulting reduced volume of solder in the joint greatly affects the mechanical strength and hence the reliability of the joint. Over and above this, excessive misalignment may interfere with adjacent components. A detailed account of these tolerances can be found in *Substrate Design Guidelines.*

The part of the solder land protruding in the longitudinal direction of the component should be at least equal to the required height of the meniscus.

Leadless SMDs

When a surface mounted leadless device is accurately placed on the solder land, and hence does not protrude from it, it should have solder meniscus along the whole periphery. If the device is misplaced (but conforms to the criteria discussed above), then the meniscus should still extend over the complete width of the connecting area situated over the solder land. If it does not, it is a major defect.

The metallization should show no signs of dissolution and should have a solder meniscus along its full length. The height of the meniscus at its centerline must be at least one third of the component metallization height for components less than 1mm (.040″) high, or 0.4mm (.016″) high for larger components. The shape of the solder fillet may be either concave or convex. The surface of the solder should be smooth and shiny, with little or no evidence of de-wetting or holes. Figure 14 shows soldered leadless SMDs.

SMDs with few short leads

Surface mounted devices with a few short leads, such as the SOT-23, SOT-89 and SOT-143, introduce new criteria. The foot and heel of the lead should be positioned within the boundaries of the solder land. A projection of half the width of the lead over the edge of the solder land constitutes a minor defect, while more than half is a major defect.

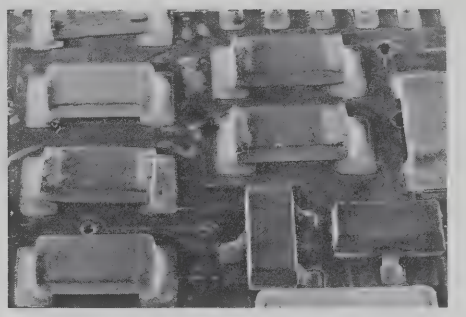


Fig. 14. Soldered leadless SMDs.

The solder should be smooth and shiny, and the sides of the lead should be fully wetted. In the case of these SMDs with a few short leads, wave soldering usually leaves a large amount of solder, surrounding the entire foot. However, the maximum amount of solder is not indicated, and the only criteria is that the joint does constitute a major defect. Figure 15 shows soldered SOT-23 devices.

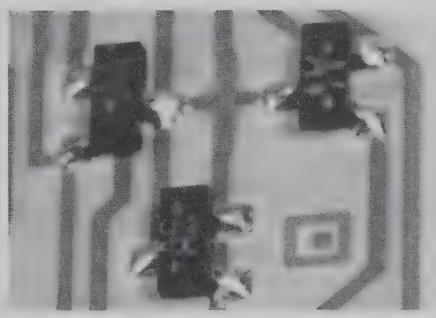


Fig. 15. Soldered SOT-23 devices.

SO IC packages

For surface mounted IC packages which have a larger lead count, for example, small-outline (SO) ICs, a projection of more than half the width of the lead is again a major defect. A projection smaller than half the width of the lead is a minor defect. Shifting

in the longitudinal direction of the lead is not a problem, as long as the whole foot of the lead is situated on the solder land.

Inspection can be confined to those areas of the lead that form the actual joint, that is, the sides and heel of the foot, and the space between the heel and the solder land. The top surface of the foot should show evidence of wetting, although an homogeneous coat is not necessary. The cut end of the foot need not be wetted, but a meniscus is usually present.

For the optimun joint, the space between the heel and the solder land should be filled with solder with a meniscus height equal to the thickness of the lead. Figure 16 shows this criteria on a cross-section through a soldered SO IC lead. The solder fillets on the sides of the foot should also be this height. In the case of projection of the leads beyond the solder lands, this requirement is valid only for the side of the lead situated on the solder land. A meniscus height, of less than half the lead thickness unacceptable.

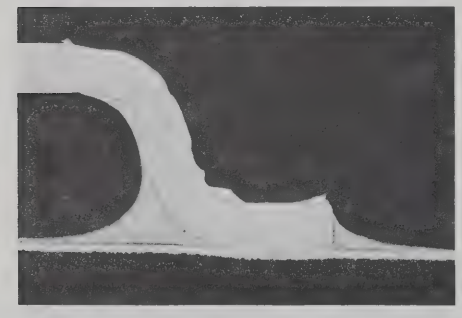


Fig. 16. Cross-section through a soldered SO IC lead.

VSO IC packages

The criteria for assessing a good soldered joint on very small outline (VSO) packages are largely the same as for the SO with regard to the meniscus height and degree of wetting. However, at minimum joint, the foot of the lead should be secured over at least three quarters of its length, and the sides of the leads are wetted over the secured length to a height equal to half the thickness of the lead. Figure 17 shows a cross-section through a soldered VSO lead and Fig. 18 shows a scanning electron microscope (SEM) photograph of well soldered VSO leads.

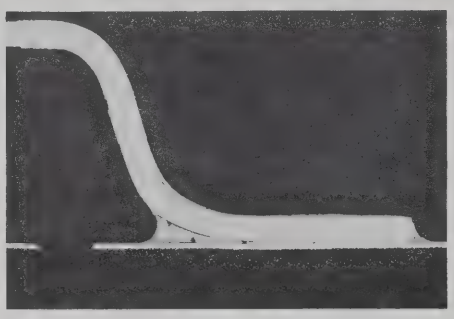


Fig. 17. Cross-section through a soldered VSO IC lead.

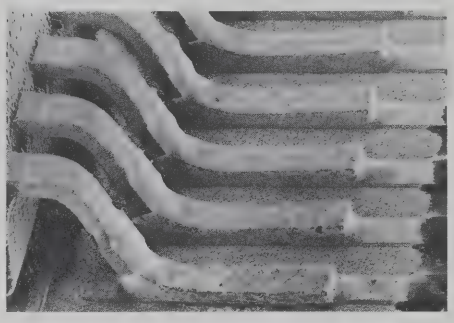


Fig. 18. Soldered VSO IC leads.

PLCC with J-leads

For ICs in plastic leaded chip carriers (PLCCs), part of the lead and its associated solder fillet will be hidden from view beneath the component. It is necessary, therefore, to assess the quality of the joint from the quantity of solder and the appearance of the fillet between the outside bend of the lead and the solder land.

In the ideal joint, the sides of the lead should be wetted and the area between the outside bend and the solder land should be filled with solder to a height equal to the thickness of the lead (see Fig. 19). A meniscus extending to a height equal to half the thickness of the lead is the acceptable minimum. In both cases, the solder should wet the entire solder land.

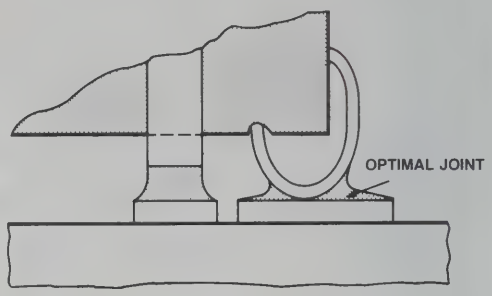


Fig. 19. Acceptable joint on a PLCC J-lead.

Chip carriers with metallized castellations

As with SOTs and SOs, the metallization of leadless ceramic chip carriers (LCCCs) should be aligned with the solder lands. Up to half a width overlap is a minor defect, more than half a width is a major defect. The whole of the metallization and the solder lands should be wetted. The solder fillet should extend to the full height of the metallization and to the edges of the land. A concave surface is indicative of good wetting beneath the component by capillary action. Figure 20 illustrates the unacceptable and acceptable volumes of solder for LCCC packages with castellated terminations.

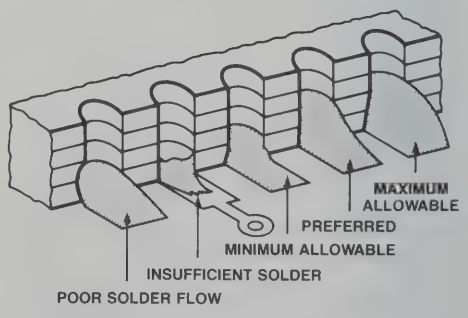


Fig. 20. Joint criteria for LCCCs with catellated connecting areas.

Inspection Systems

Although visual inspection with the aid of a magnifier is the most cost-effective method, and adequate for most consumer products, the choice of system may well be influenced by criteria other than cost, for example, high throughput speed or ultra-high reliability.

It is necessary, therefore, to consider the following factors when evaluating an inspection system:

Speed of inspection: the higher the throughput, the more cost effective the system.

Operator fatigue: results in lack of concentration, hence more defects get through, or good joints get rejected.

Judgment: consistency in operator judgment is difficult to maintain and the human factor should be kept to a minimum.

Resolution: high resolution can often be at the expense of other factors.

Parts manipulation: the more automation the better. Excessive handling increases the probability of mechanical or electro-static damage.

Depth of field: for optical systems only. Evaluation is easier if the whole joint can be viewed at once.

Field of view: should be as large as possible to allow for a maximum number of joints to be viewed with a minimum of manipulation.

ADVANTAGES AND DISADVANTAGES OF INSPECTION SYSTEMS

SYSTEM TYPE	ADVANTAGES	DISADVANTAGES
Binocular microscope	• Easy manipulation • Low cost • Good depth of field • Good field of view	• High operator fatigue • Good judgment required • Low inspection speed
Video systems	• High inspection speed • Lower operator fatigue • Reasonable resolution • Reasonable field of view	• Good judgment required • Shallow depth of field • Poor parts manipulation
X-ray inspection	• High resolution • Good judgment not needed • Good field of view • Can see hidden defects	• Low inspection speed • High cost of system • Poor parts manipulation • High level of operator training
Laser inspection	• High resolution • Good judgment not needed • Can see some hidden defects	• Very low inspection speed • High cost of system • Requires programming

Component and Substrate Solderability

An Introduction

SMD technology, as forecast, is continuing to sweep through the electronics industry, particularly in the very competitive consumer field. By using highly automated component-placement machines, and by optimizing the process parameters of new-generation mass-soldering equipment, the promise that SMD technology can produce densely packed, reliable and cost-effective substrates is being fulfilled.

But, as with any emergent technology, problems can occur, especially during the learning phase, and production engineers may well find that they are having to devote a significant part of their time to the removal of production-line bottle necks caused by a need for rework. One area where many of these bottle necks occur is during soldering. It is here that the skills of the designer and the production engineer unite to produce a quality product. This is also the area where component and substrate solderability, or the lack of it, becomes apparent.

In theory, practically every metal can be soldered, given an active enough flux, a high enough temperature, and a long enough dwell-time. In practice, however, as far as electronic circuits are concerned, the flux must be only mildly activated, soldering temperatures must be relatively low, and dwell-times kept as short as possible. So good, solderable components must be offered to meet this criteria.

A mildly activated flux will make post-soldering cleaning easier, or even unnecessary, and minimize corrosion problems. Relatively low soldering temperatures and short dwell-times will prevent damage to both substrates and SMDs. It is, therefore, essential that substrate and components have optimum solderability before assembly. This publication presents an evaluation of the solderabililty of SMDs and substrates.

Aspects of Solderability

The solderability of components and substrates can be defined by their suitability for an industrial soldering process. It is determined by:

Thermal demand—the thermal aspects of component or substrate must allow for heating of the joint area to the desired soldering temperature within the time available without adversely affecting component of substrate.

Wettability—the nature of the component metallization, or conductor, must be such that the surface is wetted with molten solder within the specified time available for soldering, without subsequent de-wetting.

Resistance to dissolution of metallization—the component and substrate metallization must be able to withstand soldering temperatures without dissolving.

During the wave soldering process, for example, the joints must be formed within a few seconds. Dwell-times of two to four seconds after preheating are common, and within these short times, the component terminations and substrate solder lands must reach a sufficiently high temperature to cause the solder to flow evenly.

SMD substrates, however, can be soldered by several different processes. For example, dual wave, infrared reflow and vapor phase reflow soldering, and each of these places specific thermal demands on the loaded substrate (these processes are covered in detail in another publication in this series titled *Soldering Techniques*). These thermal demands must be evaluated during the design stage, and component/substrate suitability established by consulting relevant specifications before starting the process of populating the substrate.

Wettability of the surfaces is affected by aging, and by the conditions of storage, transit, and handling, and therefore, more under the control of the user. Communication between manufacturer and user via standards and specifications, with regard to protection, storage, and packaging, is an important factor in ensuring that components and substrates are at a sufficient level of wettability at the start of the soldering process.

The dissolution of the component metallization during the soldering process can cause problems. SMDs in particular, must be highly resistant to dissolution, for if the metallization is lost into the solder, the integrity of the joint will be seriously affected. It is the metal used for plating the component metallization that determines the rate of dissolution.

SMD Solderability

The smaller dimensions of SMDs, together with the trend toward blister-tape packaging, makes component solderability testing by the user a difficult problem, one that has yet to be standardized. The simple globule test, as used for leaded components cannot be applied to SMDs, and quantitative analysis using the wetting balance method is impractical, owing to the very small areas of metallization.

Should the user wish to carry out solderability tests, he must, at present, rely on dipping the component vertically into molten solder, followed by a visual inspection of the terminations using a stereoscopic microscope with between ×10 and ×20 magnification. Good solderability usually requires that 95 percent of the metal surfaces are wetted by the molten solder during a dwell-time of approximately two seconds at 235°C. Figure 1 shows the areas to be examined for some typical SMD packages.

For leadless SMDs with metallized electrodes, the dipped surface should be covered with a bright solder coating with no more than small amounts of scattered imperfections (such as pinholes, non-wetted or de-wetted areas). Attention should be given to quality of the coating (appearance of the surface), and attack of the metallization (any decrease in area). Figure 2 shows an evaluation of the solderability of leadless SMDs.

Surface mounted components with short leads, such as SO ICs with gull-wing leads, have the leads divided into three regions, each with different requirements. Shown in Figure 3, the requirements for a typical leaded device are as follows:

Region A—side faces, underside and outside bend (to a height above the underside equal to the material thickness). The highest requirements are posed for these surfaces and they shall be covered with a smooth and bright coating with no more than small amounts of scattered imperfections. These imperfections shall not be concentrated in one area.

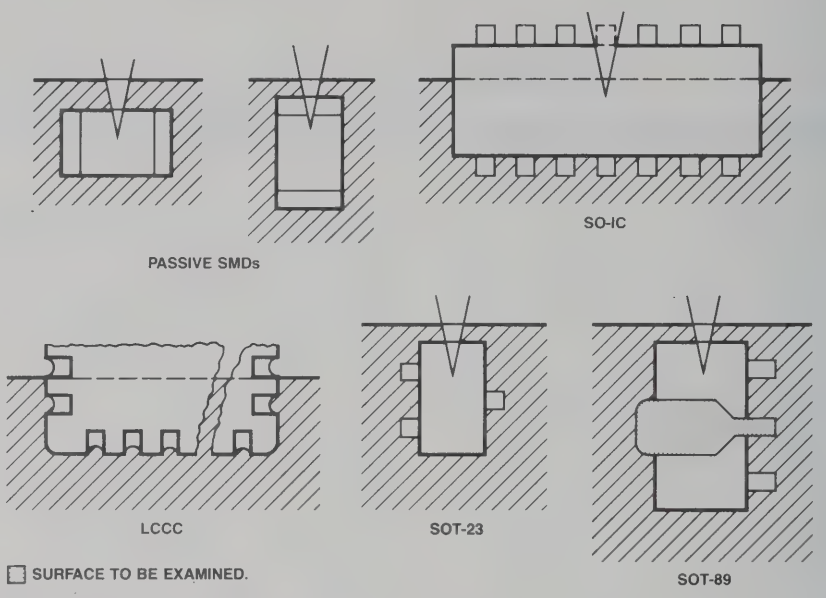


Fig. 1. Examples of immersion showing areas to be examined.

Region B—upperside of the termination. After dipping, the surface should be visibly wetted by solder. The requirements of a homogeneous coating is not necessary here.

Region C—underside of lead (except that in region A) and the non-coated cut end. For these surfaces, no requirements are posed.

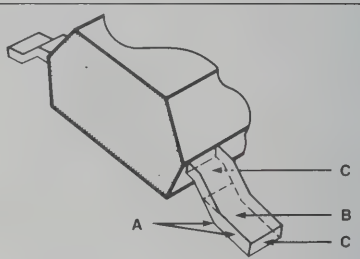


Fig. 3. Regions on a gull-wing leaded device. Solderability requirements differ for each.

Figures 4 and 5 show an evaluation of the solderability of SOT leads and SO IC leads respectively.

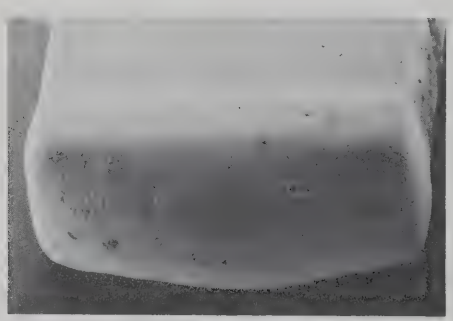


Fig. 2(a). Leadless SMD—GOOD solderability, though a few irregularities are visible.

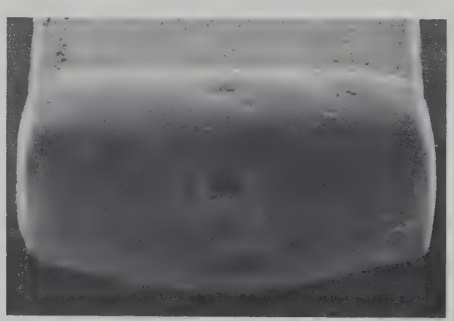


Fig. 2(b). Leadless SMD—ACCEPTABLE solderability, less than 5% of the area is not wetted.

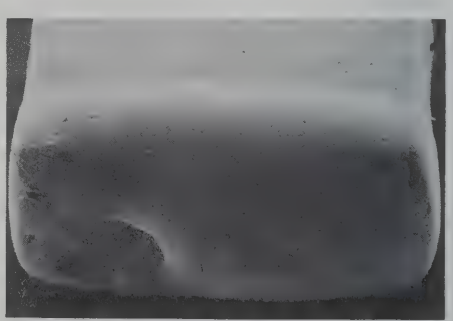


Fig. 2(c). Leadless SMD—UNACCEPTABLE solderability, more than 5% of the area is not wetted.

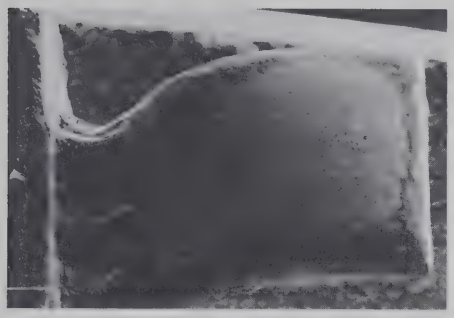


Fig. 4(a). SOT lead—good solderability, good coating on both foot and sides of the lead.

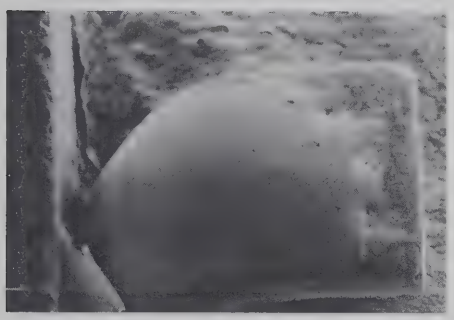


Fig. 4(b). SOT lead—unacceptable solderability, more than 5% dewetting on the toe.

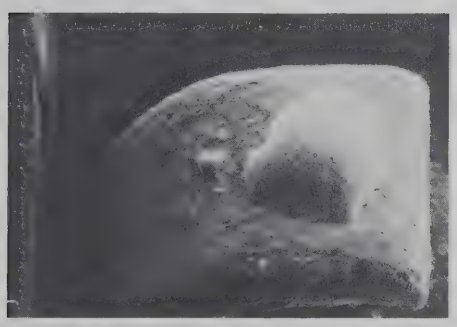


Fig. 4(c). SOT lead—very poor solderability, the foot shows a large degree of non-wetting.

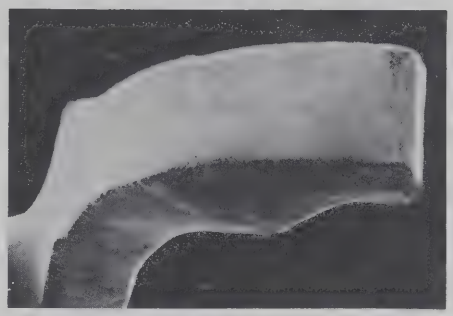


Fig. 5(a). SO IC lead—acceptable solderability, though some spots are visible where the coating is not ideal.

Fig. 5(b). SO IC lead—unacceptable solderability, more than 5% dewetting on the heel.

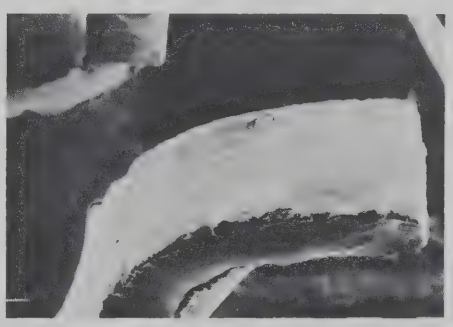


Fig. 5(c). SO IC lead—unacceptable solderability, more than 5% dewetting on the foot.

It can be expected that this method will eventually be included in the relevant standards, such as IEC 68-2-20. It is to these existing standards that manufacturers, such as Philips, test their components to ensure optimum solderability at the time of delivery.

The three factors having the most influence on component solderability are the materials used for the terminations, the conditions of storage, and the component's ability to survive at the soldering temperature. Philips, for example, uses mainly platinum or silver-palladium plating, or tin/lead plated copper, and includes maximum soldering temperatures and dwell-times in component specifications.

Substrate Solderability

The conductors for electronic circuits on printed boards are usually formed by the subtractive method, from copper sheet bonded to the substrate. This is done by preserving the conductor pattern with an etch resist, and then etching away the unwanted copper. Although copper has good wettability when the surface is freshly made, storage and handling will cause rapid deterioration unless some form of protection is provided. Some manufacturers plate the conductors with a readily wettable tin/lead alloy. In this process, the electro-deposited tin/lead layer also acts as an etch resist.

Other forms of protection, such as plating with noble metals, or covering by an organic film, are also used. Packaging in gas-tight bags is also common practice.

Protective Coatings

The types of coating applied to substrates to ensure continued wettability are generally either fusible or soluble. Fusible coatings, deposited either by electroplating with tin/lead, or coating with molten solder, will remelt and mix with the molten solder during the soldering process (see Figure 6).

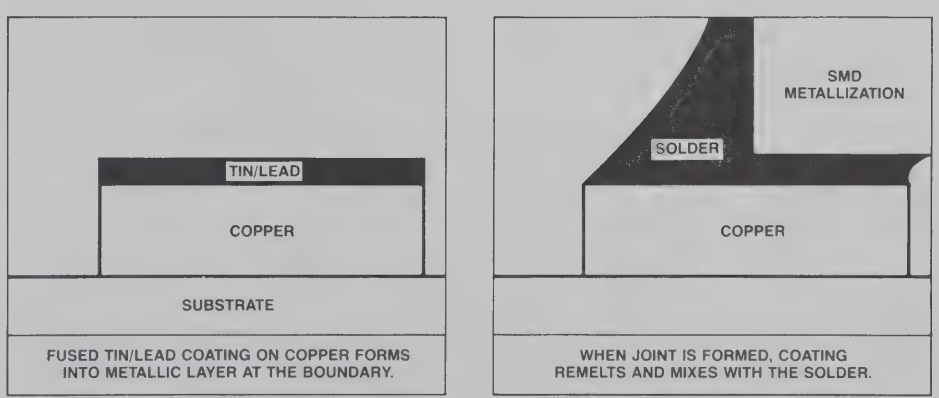


Fig. 6. A fusible protective coating remelts and mixes with the molten solder during soldering.

Soluble coatings may be either of electro-deposited noble metal, that is, gold, silver, platinum or palladium, which will dissolve into the molten solder (see Figure 7), or of an organic nature which will be dissolved by, or will mix with, the flux.

Fusible Coatings

Electro-Plated Tin/Lead

This method is used mainly in the production of substrates by the pattern plating process. A plating mask is applied over the unwanted areas of copper. The exposed pattern is electro-plated with copper, and then tin/lead. When the mask is removed, the tin/lead deposit serves as a resist during the etching process (see Figure 8). The plating may then be reflowed using hot liquid, hot air or IR radiation, to restore its wettability.

Reflowing the electro-plated tin/lead layer fuses it and forms an intermetallic zone of a copper/tin alloy at the boundary, the thickness of which is a function of temperature and time. As this copper/tin intermetallic layer has poor solderability, it is desirable to keep its thickness to a minimum, so reflowing the electro-plated tin/lead is best avoided if possible.

The electro-plated tin/lead coating, if correctly applied to a clean substrate, can provide good wettability without fowing, if storage and transit conditions are not too humid. Substrates coated in this way give a good indication of future wettability, and if showing no de-wetted or non-wetted areas, will retain it for an appreciable time.

However, with this practice, bridging problems can arise during wave soldering when the circuit resolution calls for very fine lines and spacing. Although a solder resist can help to a certain extent, the tin/lead layer beneath the resist can remelt during soldering, causing it to wrinkle and blister (as shown in Figure 9). Not only does this spoil the appearance of the finished substrate, but particles of the resist may fall off and contaminate the solder bath.

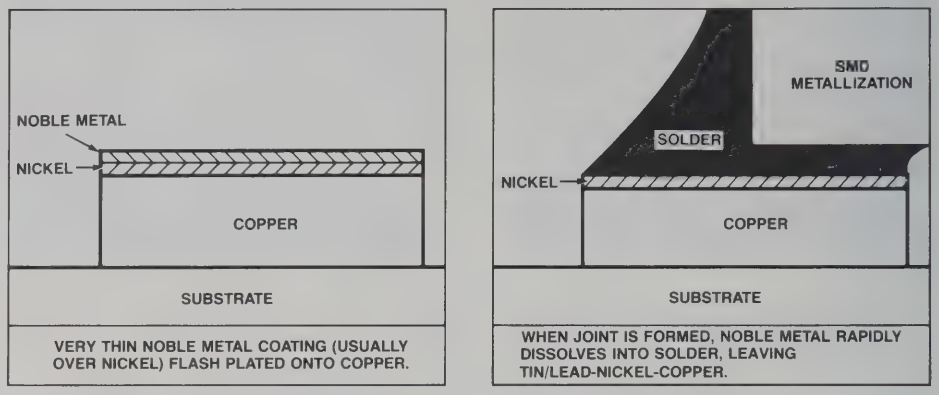


Fig. 7. A soluble protective coating dissolves into the molten solder (or into the flux, in the case of organic coatings) during the soldering process.

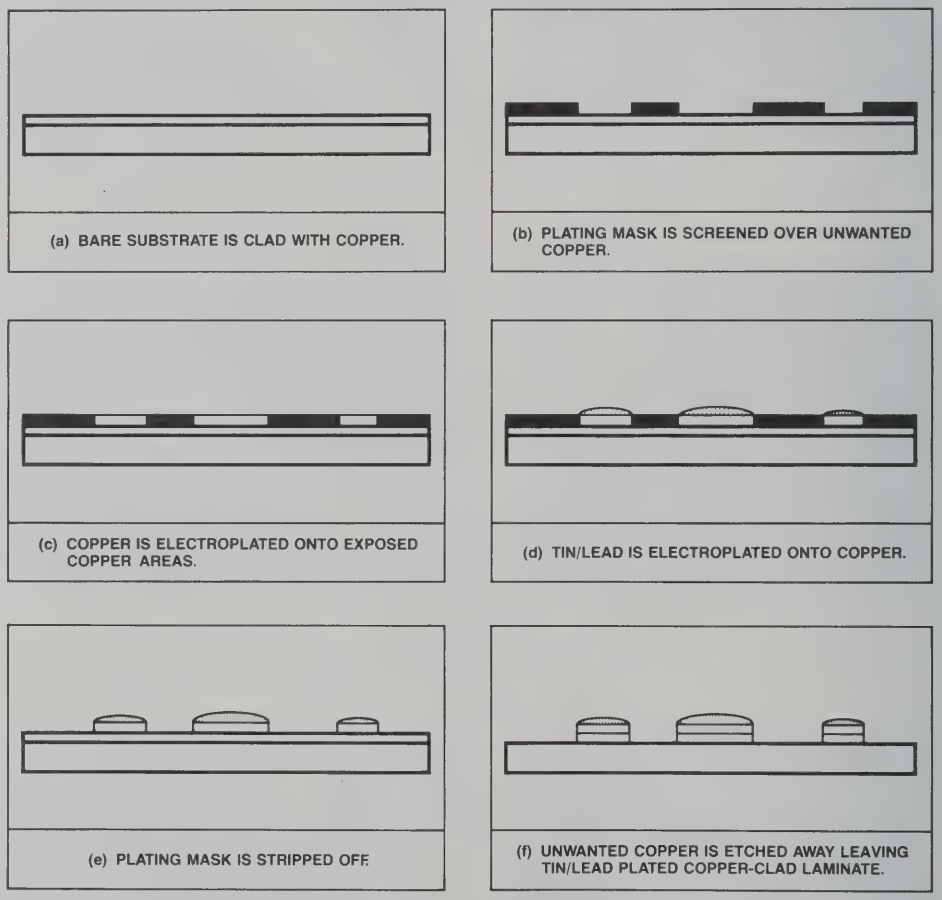

(a) BARE SUBSTRATE IS CLAD WITH COPPER.
(b) PLATING MASK IS SCREENED OVER UNWANTED COPPER.
(c) COPPER IS ELECTROPLATED ONTO EXPOSED COPPER AREAS.
(d) TIN/LEAD IS ELECTROPLATED ONTO COPPER.
(e) PLATING MASK IS STRIPPED OFF.
(f) UNWANTED COPPER IS ETCHED AWAY LEAVING TIN/LEAD PLATED COPPER-CLAD LAMINATE.

Fig. 8. The subtractive pattern plating process.

Flux may also become trapped in cracks in the resist, leading to cleaning or corrosion problems. To over-

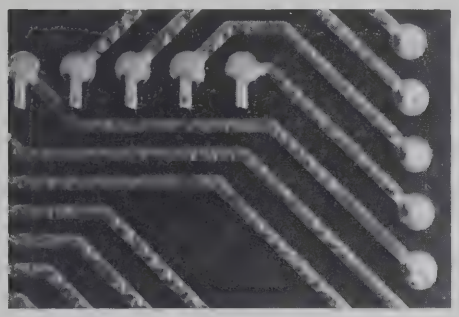


Fig. 9. Wrinkling of the solder resist coat caused by melting of the solder plating on the conductors during soldering.

come these problems, it is possible to strip off the tin/lead layer after etching and apply a solder resist directly onto the bare copper. This is followed by solder-coating the lands, and levelling the solder, usually with hot air or liquid.

Solder Coating

This process involves applying a solder resist, and then dipping the substrate, usually vertically, into molten eutectic solder for a pre-determined dwell-time. During rapid withdrawal, both sides of the substrate are exposed to either high pressure hot air or liquid. This removes excess solder and clears any plated-through holes. The result is a bright, uniform solder layer on the conductors and on the walls of plated-through holes.

The thickness of the coat is determined by the operating parameters of the machine, such as speed of withdrawal, air or liquid temperature, and the flow rate. In general, coated and levelled substrates maintain good wettability over long periods.

Solder coating and levelling also produces the copper/tin intermetallic layer, and the levelling process results in a convex meniscus of solder in the land as shown in Figure 10. When plated-through holes are present (as in mixed prints), this results in a very thin layer of solder at the edges of the holes, exposing the intermetallic layer, and wettability becomes inadequate soon after fusion (see Figure 11). During subsequent wave soldering, this lack of wettability can prevent solder flowing past the upper edges of the hole, resulting in non-wetting of the upper solder lands.

The meniscus effect has other drawbacks, particularly in SMD assembly.

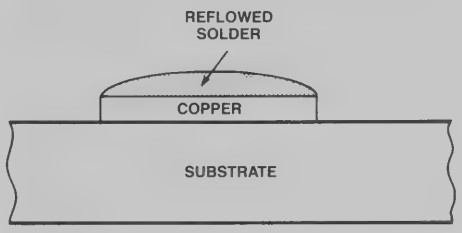


Fig. 10. Convex meniscus of solder on copper land.

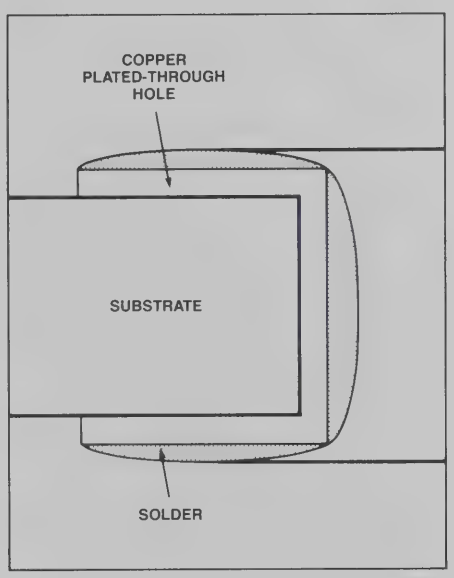


Fig. 11. Reflowed or leveled solder coating in a metallized hole showing the reduced layer thickness at the corner exposing the intermetallic layer.

It can, for example, raise the SMD above the adhesive dot, resulting in a poor bond as shown in Figure 12 (adhesive considerations are covered in detail in another publication in this series titled *Adhesive Application And Curing*). This problem is compounded as small solder lands develop a higher solder meniscus than larger lands, further complicating the adhesive dot height criteria. And as a convex meniscus provides a very small point of contact, the device may slip off-center of the solder land.

Levelling also has other limitations. Hot air levelling is an inherently dirty process, since air under pressure will inevitably blow flux and dross around. This, together with the high heat-levels developed within these systems, means that the operator must spend a significant amount of time cleaning the machine to ensure that the solder-coat thickness is uniform and consistent.

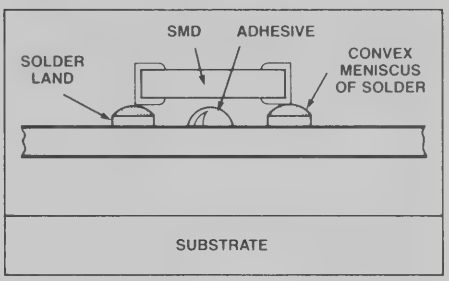


Fig. 12. Meniscus can prevent SMD making contact with the adhesive dot.

Liquid levellers on the other hand, at least those that use hot oil, can contaminate the substrate material by oil impregnation. To overcome this, machines are available employing fluorocarbon liquids or water soluble fluids. Levelling processes, whether using air or liquid, must always be followed by cleaning, because of the higher than normal activity of the flux used.

Solder Land Contamination

Whichever method is used to provide the protective layer, great care must

be taken during the application of the solder resist. The slightest contamination by the solder resist of the areas to be soldered, either by mis-registration of the solder resist pattern or "bleeding" of the resist, renders these areas irreversibly unsolderable, and usually results in the scrapping of the substrate.

Another problem which seriously affects the solderability of substrates is that of the adhesive used for bonding the SMDs bleeding onto the solder land. Many commercial adhesives are almost transparent when forming very thin layers, and if such a layer spreads onto the solder land, it renders it unsolderable. Therefore, adhesives of the correct viscosity must be used and placement must be very accurate.

Soluble Coatings

Flash Plating

Under certain conditions, soluble coatings are applied to improve the wettability of the conductors, or to provide protection against contamination during handling. Some substrates and components have to satisfy special requirements other than good solderability; requirements such as very good electrical contact, or very low electrical resistance. The conductors on these substrates are sometimes plated with a very thin layer, or 'flash' of noble metal.

When these metals are used, it is customary to plate on an intermediate layer of nickel to reduce contact resistance and to enable a thinner layer of expensive noble metal to be used without sacrificing wettability.

The cleanliness and general condition of the substrate is very important to the plating process. During soldering, the very thin layer of noble metal will dissolve rapidly into the molten solder, and, although the coated surface will readily wet during soldering, if the underlying layer is not absolutely clean and free from oxides, the surface will quickly de-wet once dissolution has occurred.

Organic Coatings

Unplated, copper-clad substrates that are going to be populated shortly after manufacture are often covered with an approximately 0.5 μm thick organic coating, based on modified colophony. This coating only protects against fingerprints and so on, it does not prevent oxidization of the underlying copper.

A film-former, such as acrylate or epoxy is usually combined with the colophony to prevent crumbling. During soldering, the colophony based coating will be dissolved and mixed with the flux. If the substrates contain plated-through holes, however, the film-former is usually omitted, as it has a tendency to remain in the holes and adversely affect the flow of solder.

Protective Packaging

Reasonably good protection against an aggressive environment can be provided by sealing the substrate for storage and transit in a polythene bag containing a dehydrator such as silica-gel. Although polythene is not gas-tight, the preservation of wettability is good, especially for substrates with coated conductors.

The best results, however, are obtained by sealing the substrates in individual bags made from laminated polythene-aluminium-polyester, and substrates stored in this way should maintain good wettability for up to two years.

Conclusion

In conclusion, the advantages of good solderability of both component and substrate can be summarized in the following points:

- Lower soldering temperatures and shorter dwell-times—prevents damage to devices or dissolution of metallization, and minimizes the thickness of intermetallic zones, thus increasing mechanical integrity and providing a stable electrical connection.
- Permits the use of a less active flux—therefore the flux residue activity is low and cleaning the substrate may be unnecessary.
- Better cost effectiveness—shorter production times owing to less re-working and repairs.

Fluxing and Cleaning

An Introduction

The adoption of mass soldering techniques by the electronics industry was prompted not only by economics, and a requirement for high throughput levels, but also by the need for a consistent standard of quality and reliability in the finished product simply unattainable with manual methods. With surface mounted device (SMD) assembly, this need is even greater.

The quality of the end-product depends on the measures taken during the design and manufacturing stages. The foundations of a high quality electronic circuit are laid with good design, and with correct choice of components and substrate configuration. It is, however, at the manufacturing stage where the greatest number of variables, both with respect to materials and techniques, have to be optimized to produce high quality soldering, a prerequisite for reliability.

Of the two most commonly used soldering techniques, wave and reflow, wave soldering is by far the most widely used and understood. Many factors influence the outcome of the soldering operation, some relating to the soldering process itself, and others to the condition of components and substrate to which they are to be attached. These must be collectively assessed to ensure high quality soldering.

And one of the most important, most neglected and least understood of these processes is the choice and application of flux. This publication outlines the fluxing options available, and discusses the various cleaning techniques that may be required, for SMD substrate assembly.

Fluxes

Populating a substrate involves the soldering of a variety of terminations simultaneously. In one operation, a mixture of tinned copper, tin/lead or gold plated nickel-iron, palladium-silver, tin/lead plated nickel-barrier, and even materials like Kovar, each possessing varying degrees of solderability, must be attached to a common substrate using a single solder alloy.

It is for this reason that the choice of the flux is so important. The correct flux will remove surface oxides, prevent reoxidization, help to transfer heat from source to joint area, and leave non-corrosive, or easily removable corrosive residues on the substrate. It will also improve wettability of the solder joint surfaces.

The wettability of a metal surface is its ability to promote the formation of an alloy at its interface with the solder to ensure a strong, low-resistance joint.

However, the use of flux does not eliminate the need for adequate surface preparation. This is very important in the soldering of SMD substrates, where any temptation to use a highly-active flux in order to promote rapid wetting of ill-prepared surfaces should be avoided because it can cause serious problems later when the corrosive flux residues have to be removed. Consequently, optimum solderability is an essential factor for SMD substrate assembly (this is covered in another publication titled *Component and Substrate Solderability*).

Flux is applied before the wave soldering process, and during the reflow soldering process (where flux and solder are combined in a solder cream). By coating both bare metal and solder, flux retards atmospheric oxidization which would otherwise be intensified at soldering temperature. In the areas where the oxide film has been removed, a direct metal-to-metal contact is established with one, low energy interface. It is from this point of contact that the solder will flow.

Types Of Flux

There are two main characteristics of flux. The first is efficacy—its ability to promote wetting of surfaces by solder within a specified time. Closely related to this is the activity of the flux, that is, its ability to chemically clean the surfaces.

The second is the corrosivity of the flux, or rather the corrosivity of its residues remaining on the substrate after soldering. This is again linked to the activity; the more active the flux, the more corrosive are its residues.

Although there are many different fluxes available, and many more being developed, they fall into two basic categories: Those with residues soluble in organic liquids, and those with residues soluble in water.

Organic Soluble Fluxes

Most of the fluxes soluble in organic liquids are based on colophony or rosin, (a natural product obtained from pine sap that has been distilled to remove the turpentine content). Solid colophony is difficult to apply to a substrate during machine soldering, so it is dissolved in a thinning agent, usually an alcohol. It has a very low efficacy, and hence limited cleaning power, so activators are added in varying quantities to increase it. These take the form of either organic

acids, or organic salts that are chemically active at soldering temperatures. It is therefore convenient to classify the colophony-based fluxes by their activator content.

Non-Activated Rosin (R) Flux

These fluxes are formed from pure colophony in a suitable solvent, usually isopropanol or ethyl alcohol. Efficacy is low and cleaning action is weak. Their uses in electronic soldering are limited to easily wettable materials with a high level of solderability. They are used mainly on circuits where no risk of corrosion can be tolerated, even after prolonged use, (implanted cardiac pacemakers for example). Their flux residues are non-corrosive and can remain on the substrate, where they will provide good insulation.

Rosin, Mildly Activated (RMA) Flux

These fluxes are also composed of colophony in a solvent, but with the addition of activators, either in the form of di-basic organic acids (such as succinc acid), or organic salts (such as dimethylammonium chloride or diethylammonium chloride). It is customary to express the amount of added activator as mass percent of the chlorine ion on the colophony content, as the activator-to-colophony ratio determines the activity, and hence the corrosivity. In the case of RMA activated with organic salts, this is only some tenths of one percent.

When organic acids are used, a higher percentage of activator must be added to produce the same efficacy as organic salts, so frequently, both salts and acids are added. The cleaning action of RMA fluxes is stronger than that of the R type, although the corrosivity of the residues is usually acceptable. These residues may be left on the substrate as they form a useful insulating layer on the metal surfaces. This layer can, however, impede the penetration of test probes at a later stage.

Rosin, Activated (RA) Flux

The RA fluxes are similar to the RMA fluxes but contain a higher proportion of activators. They are used mainly when component or substrate solderability is poor and corrosion-risk requirements are less stringent. However, as good solderability is considered essential for SMD assembly, highly activated rosin fluxes should not be necessary. The removal of flux residues is optional; usually dependent upon the working environment of the finished product and the customers requirements.

Water Soluble Fluxes

The water soluble fluxes are generally used to provide high fluxing activity. Their residues are more corrosive and more conductive than the rosin-based fluxes, and consequently must always be removed from the finished substrate. Although termed water soluble, this does not necessarily imply that they contain water; they may also contain alcohols or glycols. It is the flux residues that are water soluble.

The usual composition of a water soluble flux is shown below.

(1) A chemically active component for cleaning the surfaces.
(2) A wetting agent to promote the spreading of flux constituents.
(3) A solvent to provide even distribution.
(4) Substances such as glycols or water soluble polymers to keep the activator in close contact with the metal surfaces.

Although these substances can be dissolved in water, other solvents are generally used, as water has a tendency to spatter during soldering. Solvents with higher boiling points, such as ethylene glycol or polyethylene glycol are preferred.

Water Soluble Fluxes With Inorganic Salts

These are based on inorganic salts such as zinc chloride or ammonium chloride or inorganic acids such as hydrochloric. Those with zinc or ammonium chloride must be followed by very stringent cleaning procedures as any halide salts remaining on the substrate will cause severe corrosion. These fluxes are generally used for non-electrical soldering. Although the hydrazine halides are among the best active fluxing agents known, they are highly suspect from a health point of view and are therefore no longer used by flux manufacturers.

Water Soluble Fluxes With Organic Salts

These fluxes are based on organic hydrohalides such as dimethylammonium chloride, cyclo hexalamine hydrochloride and aniline hydrochloride, and also on the hydrohalides of organic acids. Fluxes with organic halides usually contain vehicles such as glycerol or polyethylene glycol, and non-ionic surface-active agents such as nonylphenol polyoxyethylene. Some of the vehicles, such as the polyethylene glycols, can degrade the insulation resistance of epoxy substrate material and, by rendering the substrate hydrophilic, make it susceptible to electrical leakage in high humidity environments.

Water Soluble Fluxes With Organic Acids

Based on acids such as lactic, melonic or citric, these fluxes are used when the presence of any halide is prohibited. However, their fluxing action is weak and high acid concentrations have to be used. On the other hand, they have the advantage that the flux residues can be left on the substrate for some time before washing without the risk of severe corrosion.

Solder Creams

For reflow soldering, both the solder and the flux are applied to the substrate before soldering and can be in the form of solder creams (or pastes), preforms, electro-deposit, or a layer of solder applied to the conductors by

dipping. For SMD reflow soldering, solder cream is generally used.

Solder cream is a suspension of solder particles in flux to which special compounds have been added to improve the rheological properties. The shape of the particles is important and normally spherical particles are used, although non-spherical particles are now being added, particularly in very fine-line soldering.

In principle, the same fluxes are used in solder creams as for wave soldering. However, due to the relatively large surface area of the solder particles (which can oxidize), more effective fluxing is required and in general solder creams contain a higher percentage of activators than the liquid fluxes. The drying of the solder paste during pre-heating (after component placement) is an important stage as it reduces any tendency for components to become displaced during soldering.

Flux Selection

Choosing an appropriate flux is of prime importance to the soldering system for the production of high quality, reliable joints. When solderability is good, a mildly activated flux will be adequate, but when solderability is poorer, a more effective, more active flux will be required. The choice of flux, moreover, will be influenced by the cleaning facilities available, and if in fact, cleaning is even feasible.

With water-soluble fluxes, aqueous cleaning of the substrate after soldering is mandatory. If thorough cleaning is not carried out, severe problems may arise in the field, due to corrosion or short circuits caused by too low a surface resistance of the conductive residues.

For rosin based fluxes, the need for cleaning will depend on the activity of the flux. Mildly activated rosin residues can, in most cases, remain on the substrate where they will afford protection and insulation. In practice, for the great majority of electronic circuits, the choice will be between an RA or an RMA rosin based flux.

Application Of Flux

Three basic factors determine the method of applying flux: the soldering process (wave or reflow), the type of substrate being processed (all-SMD or mixed print), and the type of flux.

For wave soldering the flux must be applied in liquid form before soldering. While it is possible to apply the flux at a separate fluxing station, with the high through-put rates demanded to maximize the benefits of SMD technology, today's wave soldering machines incorporate an integral fluxing station prior to the pre-heat stage. This enables the pre-heat stage to be used to dry the flux as well as pre-heat the substrate to minimize thermal shock.

The most commonly used methods of applying flux for wave soldering are by foam, wave or spray.

Foam Fluxing

Foam flux is generated by forcing low pressure clean air through an aerator immersed in liquid flux (see Fig. 1). The fine bubbles produced by the aerator are guided to the surface by a chimney-shaped nozzle. The substrates are passed across the top of the nozzle so that the solder side comes in contact with the foam and an even layer of flux is applied. As the bubbles burst, flux penetrates any plated-through holes in the substrate.

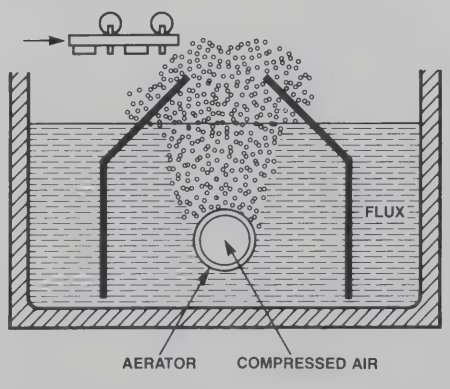


Fig. 1 Schematic diagram of foam fluxer.

Wave Fluxing

A double-sided wave can also be used to apply flux, where the washing action of the wave deposits a layer of flux on the solder side of the substrate (see Fig. 2). Wave-height control is essential and a soft, wipe-off brush should be incorporated on the exit side of the fluxing station to remove excess flux from the substrate.

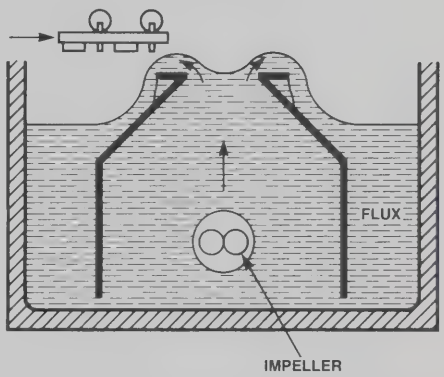


Fig. 2 Schematic diagram of wave fluxer.

Spray Fluxing

Several methods of spray fluxing exist; the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate (see Fig. 3). Four parameters affect the amount of flux deposited: conveyor speed, drum rotation, air pressure and flux density. The thickness of the flux layer can be controlled using these parameters, and can vary between 1 and 10 μm.

The advantages and disadvantages of these three flux application techniques are outlined in Table 1.

Flux Density

One of the main control factors for fluxes used in machine soldering is

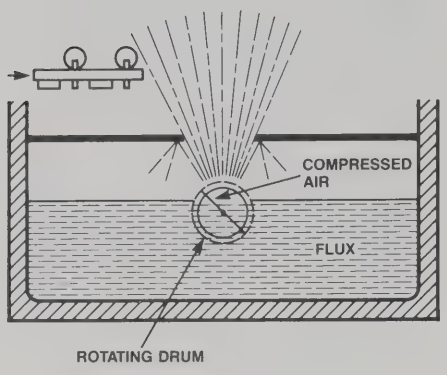


Fig. 3 Schematic diagram of spray fluxer.

Table 1. Advantages And Disadvantages Of Flux Application Methods

Method	Advantages	Disadvantages
Foam fluxing	• Compatible with continuous soldering process. • Foam crest height not critical. • Suitable for mixed print substrates.	• Not all fluxes have good foaming capabilities. • Losses through evaporation may be appreciable. • Prolonged pre-heating because of high boiling point of solvents.
Wave fluxing	• Can be used with any liquid flux. • Compatible with continuous soldering process. • Suitable for densely populated mixed print.	• Wave crest height is critical to ensure good contact with bottom of substrate without contaminating the top.
Spray fluxing	• Can be used with most liquid fluxes. • Short pre-heat time if appropriate alcohol solvents are used. • Layer thickness is controllable.	• High flux losses due to non-recoverable spray. • System requires frequent cleaning.

the flux density. This provides an indication of the solids content of the flux, and is dependent on the nature of the solvents used. Automatic control systems, which monitor flux density and inject more solvent as required, are commercially available and it is relatively simple to incorporate them into the fluxing system.

Pre-Heating

Pre-heating the substrate before soldering serves several purposes. It dries the flux to evaporate most of the solvent, thus increasing the viscosity. If the viscosity is too low, the flux may be prematurely expelled from the substrate by the molten solder. This can result in poor wetting of the surfaces, and solder spatter.

Drying the flux also accelerates the chemical action of the flux on the surfaces, and so speeds up the soldering process. During the pre-heating stage, substrate and components are heated to between 80° and 90°C (solvent based fluxes) or to between 100° and 110°C (water based systems). This reduces the thermal shock when the substrate makes contact with the molten solder, and minimizes any likelihood of the substrate warping.

The most common methods of pre-heating are convection heating with forced air, radiation heating using coils, infra-red quartz lamps or heated panels, or a combination of both convection and radiation. The use of forced air has the added advantage of being more effective for the removal of evaporated solvent. Optimum pre-heat temperature and duration will depend on the nature and design of the substrate and the composition of the flux.

Figure 4 shows a typical method of pre-heat temperature control. The desired temperature is set on the control panel and the microprocessor regulates pre-heater no. 1 to provide approximately 60 percent of the required heat. The IR detector scans the substrate immediately following no. 1 heater and reads the surface temperature. By taking into account the surface temperature, conveyor speed, and the thermal characteristics of the substrate, the microprocessor then calculates the amount of additional heat required to be provided by heater no. 2 in order to attain the pre-set temperature. In this way, each substrate will have the same surface temperature on reaching the solder bath.

Post-Soldering Cleaning

Now that world-wide efforts in both commercial and industrial electronics are converting old designs from conventional assembly to surface mounting, or a combination of both, it can also be expected that high volume cleaning systems will convert from in-line aqueous cleaners to in-line solvent cleaners or in-line saponification systems (a technique that uses an alkaline material in water to react with the rosin so that it becomes water soluble). These systems may, however, become subject to environmental objections, and new governmental restrictions on the use of halogenated hydrocarbons.

The major reason for this is that the water soluble flux residues, containing a higher concentration of activators, or showing hygroscopic behavior, are much more difficult to remove from SMD populated substrates than rosin based flux residues. This is primarily because the higher surface tension of water, compared to solvents, makes it difficult for the cleaning agents to penetrate beneath SMDs, especially the larger ones, with their greatly re-

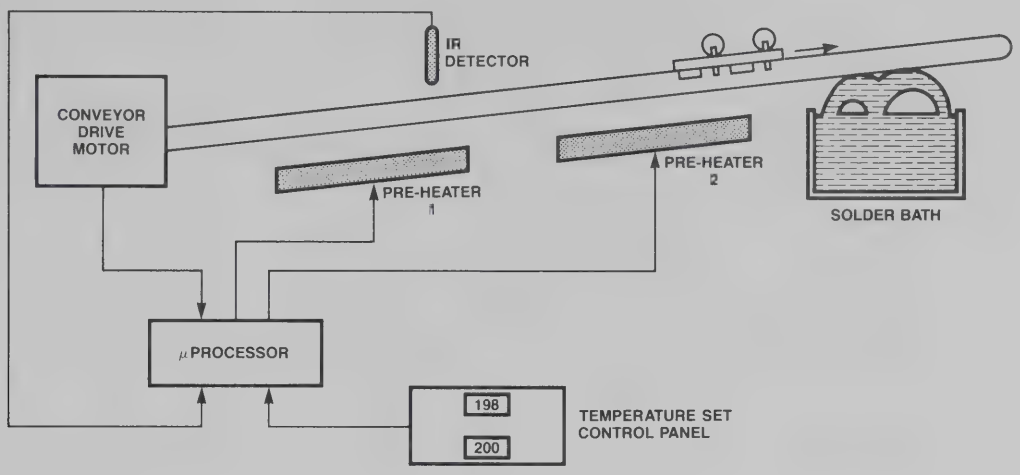


Fig. 4 Schematic diagram of a typical controlled pre-heat system.

duced off-contact distance (the distance between component and substrate).

Post-soldering cleaning removes any contamination, such as surface deposits, inclusions, occlusions or absorbed matter which may degrade to an unacceptable level, the chemical, physical or electrical properties of the assembly. The types of contaminant on substrates that can produce either electrical or mechanical failure over short or prolonged periods are shown in Table 2.

All these contaminants, irrespective of their origin fall into one of two groups, polar and non-polar.

Polar Contaminants

These are compounds that dissociate into free ions which are very good conductors in water, quite capable of causing circuit failures. They are also very reactive with metals and produce corrosive reactions. It is essential that polar contaminants are removed from the substrates.

Non-Polar Contaminants

These compounds do not dissociate into free ions or carry an electrical current and are generally good insulators. Rosin is a typical example of a non-polar contaminant. In most cases, non-polar contamination does not contribute to corrosion or electrical failure and may be left on the substrate. They may however, impede functional testing by probes and prevent good conformal coat adhesion.

Table 2. Substrate Contaminants

Contaminant	Origin
Organic compounds	Fluxes, solder mask
Inorganic insoluble compounds	Photo-resists, substrate processing
Organo-metallic compounds	Fluxes, substrate processing
Inorganic soluble compounds	Fluxes
Particle matter	Dust, fingerprints

Solvents

The solvents currently used for the post-soldering cleaning of substrates are normally organic based and are covered by three classifications: hydrophobic, hydrophillic, and azeotropes of hydrophobic/hydrophillic blends.

Azeotropic solvents are mixtures of two or more different solvents which behave like a single liquid in so much that the vapor produced by evaporation has the same composition as the liquid, which has a constant boiling point between the boiling points of the two solvents that form the azeotrope. The basic ingredients of the azeotropic solvents are combined with alcohols and stabilizers. These stabilizers, such as nitromethane, are included to prevent corrosive reaction between the metallization of the substrate and the basic solvents.

Hydrophobic solvents do not mix with water at concentrations exceeding 0.2% and consequently have little effect on ionic contamination. They can be used to remove non-polar contaminants such as rosin, oils and greases.

Hydrophillic solvents do mix with water and can dissolve both polar and non-polar contamination, but at different rates. To overcome these differences, azeotropes of the various solvents are formulated to maximize the dissolving action for all types of contamination.

Solvent Cleaning

Two types of solvent cleaning systems are in use today, batch and conveyorized systems; either can be used for high-volume production. In both systems, the contaminated substrates are immersed in the boiling solvents, and ultrasonic baths or brushes may also be used to further improve the cleaning capabilities.

The washing of rosin based fluxes offers advantages and disadvantages. Washed substrates can usually be inserted into racks easier, as there will be no residues on their edges; test probes can make better contact without a rosin layer on the test points, and the removal of the residues makes it easier to visually examine the soldered joints. On the other hand, washing equipment is expensive, and so are the solvents, and some solvents present a health or environmental hazard if not correctly dealt with.

Aqueous Cleaning

For high-volume production, special machines have been developed in which the substrates are conveyor fed through the various stages of spraying, washing, rinsing and drying. The final rinse water is blown from the substrates to prevent any deposits from the water being left on the substrate.

Where water soluble fluxes have been used in the soldering process, substrate cleaning is mandatory. For the rosin based fluxes it is optional and is often at the discretion of the customer.

Conformal Coatings

A conformal, or protective coating on the substrate, applied at the end of processing prevents or minimizes the effects of humidity and protects the substrate from contamination by airborne dust-particles. Substrates that are to be provided with a conformal coating (dependent on the environmental conditions to which the substrate will be subjected) must first be washed.

Environmental And Ecological Aspects Of Fluxes And Solvents

Fumes and vapors produced during soldering processes, or during cleaning, will not, under normal circumstances, present a health hazard, providing relevant health and safety regulations are observed.

Fumes originating from colophony can cause respiratory problems, so an efficient fume-extraction system is essential. The extraction system must cover the fluxing, pre-heating and soldering stations, remain operational for at least one hour after machine shutdown, and conform to local regulations. Today, the problem of noxious fumes is unlikely to concern the cleaning station as all commercial systems are equipped to condense the vapors back into the system. In the future, however, it can be expected that a much lower degree of escape of noxious fumes from any system will be allowed, and all systems may have to be reviewed.

Certain fluxes, particularly some water soluble ones, contain highly aggressive substances, and must not be allowed to come into contact with the skin or eyes. Any contamination should immediately be removed with plenty of clean, fresh water. De-ionized water should also be readily available as an eye-wash. Should contamination occur, a qualified medical practitioner should be consulted. Protective clothing should be worn during cleaning or maintenance of the fluxing station.

Conclusions

SMD technology imposes tougher restraints on fluxing and cleaning of substrate assemblies. Traditionally, rosin based fluxes have been used in electronic soldering where residues were considered "safe" and could be left on the board. However, increased SMD packing density, fine-line tracks and more rigid specifications have resulted in changes to this basic philosophy.

There is now a demand for surfaces free from residues; test probes are more efficient when they do not have to penetrate rosin flux residues, and conformal coating and board inspection benefit from the absence of such residues.

Cleaning also poses problems for SMD substrates. The close proximity of component and substrate means that solvents cannot effectively clean beneath devices. Components must also be compatible with the cleaning process. They must, for example, be resistant to the solvents used and to the temperatures of the cleaning process. They must also be sealed to prevent cleaning fluids from entering the devices and degrading performance.

So eliminating the need for cleaning is better than poor or incomplete cleaning. And in a well balanced system, mildly activated rosin based fluxes, leaving only non-corrosive residues, can be successfully used for SMD substrate soldering without subsequent cleaning.

Much research is at present being carried out into fluxes and solder creams; for example, the production of synthetic resin, with superior qualities to colophony at a lower cost. Another area of research is that of solder creams with non-melting additives, such as lead or ceramic spheres, that increase the distance between component and substrate, thus making it easier for cleaning fluids to penetrate beneath the component. It also increases the joint's ability to withstand thermal cycling.

Rosin-free and halide-free fluxes are also being developed with similar activities to conventional rosin-based fluxes. These new types will combine the "safety" of rosin fluxes with easier removal in conventional solvents. Using non-polar materials, ionizable or corrosive residues are eliminated, and the need for cleaning immediately after soldering is avoided.

Test and Repair

An Introduction

The key questions that must be asked of any electronic circuit are "does it work, and will it continue to do so over a specified period of time?" Until zero-defect soldering is achieved, and all components are guaranteed serviceable by the vendors, manufacturers can only answer these questions by carrying out some form of test on the finished product.

The types of tests, and the depth to which they are carried out, are determined by the complexity of the circuit and the customer's requirements. The amount of rework to be performed on the circuit will depend on the results of these tests and the degree of reliability demanded. The criteria is true of all electronic assemblies, and the test engineer must formulate test schedules accordingly.

Substrates loaded with surface mounted devices (SMDs), however, pose additional problems to the test engineer. The devices are much smaller, and substrate population density is greater, leading to difficulty in accessing all circuit nodes and test points. Also SMD substrate layout designs often have fewer via and component lead holes so test points may not all be on one side of the substrate, and double-sided test fixtures become necessary.

To achieve the high throughput rates made possible by using highly automated SMD placement machines and volume soldering techniques, automatic testing becomes a necessity. Visual inspection of the finished substrate by trained inspectors can normally detect about 90 percent of defects. With the correct combination of automatic test equipment, the remainder can be eliminated. In this publication, we hope to provide the manufacturer with information to enable him to evaluate and select the best combination of test equipment and the most effective test methods for his product.

Bare-Board Testing

Although SMD substrates will undoubtedly be smaller than conventional through-hole substrates, and have less space between conductors, the principles of bare-board testing remain the same. Many of the testers already in use can, with little or no modification, be used for SMD substrates. As this is already a well-established and well-documented practice, it will not be discussed further in this publication, but it is recommended that bare-board testing is always used as the first step in assuring board integrity.

Post-Assembly Testing

Testing densely populated substrates is no easy task, as the components may occupy both sides of the board and cover many of the circuit nodes (see Fig. 1 for the three main types of SMD populated substrates). Unlike conventional substrates, on which all test points are usually accessible from the bottom, SMD assemblies must be designed from the start with the siting of test points in mind. Probing SMD substrates is particularly difficult owing to the very close spacing of components and conductors.

Mixed print or all-SMD assemblies with components on both sides further aggravate the testing problems, as not all test points are present on the same side of the board. Although two-sided test fixtures are feasible, they are expensive and require considerable time to build.

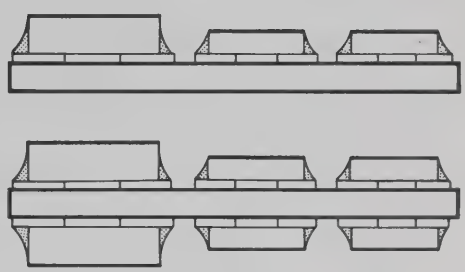


Fig. 1(a). Type I — Total surface mount (all-SMD) substrates.

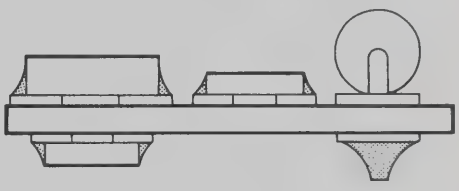


Fig. 1(b). Type IIA — Mixed print (double sided) substrate.

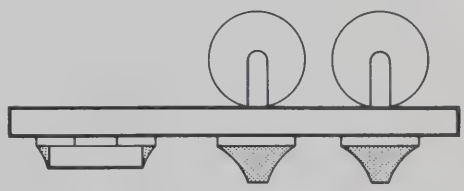


Fig. 1(c). Type IIB — Mixed print (underside attachment) substrate.

The application of a test probe to the top of an SMD termination could damage it, and probe pressure on a poor or open solder joint can force contact and thus allow a defective joint to be assessed as good. Fig. 2(a) illustrates the recommended siting of test points close to SMD terminations,

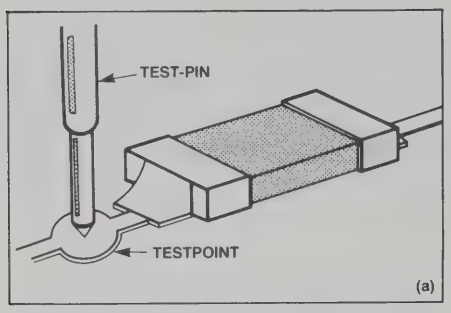


Fig. 2(a). Recommended location of test points close to SMDs.

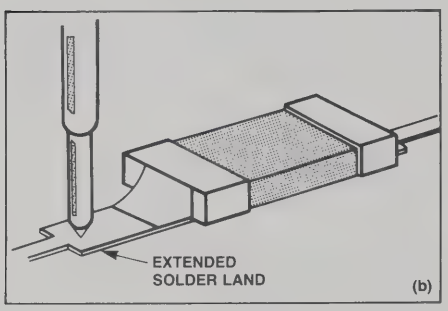


Fig. 2(b). Acceptable, though not recommended, location of test points close to SMDs.

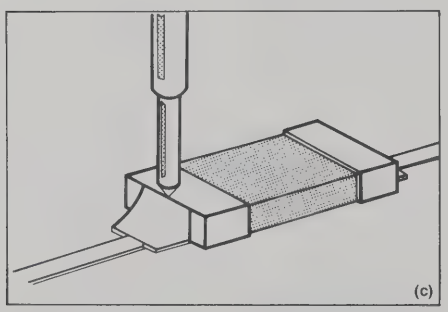


Fig. 2(c). Unacceptable location of test points close to SMDs.

and Fig. 2(b) shows an alternative, though not recommended, option. Here, problems could arise when reflow soldering (solder migrating from the joint) unless the test point area is separated from the solder land area with a stripe of solder resist. Excessive mechanical pressure caused by too many probes concentrated in a small area may also result in substrate damage.

It is good practice for substrates to have test points on a regular grid so that conventional, rather than custom, testers may be used. If the substrate has tall components or heatsinks, the test points must be located far enough away to allow the probes to make good contact. All test points should be solder coated to provide good electrical contact. Via holes may also be used as test points but the holes must be filled with solder to prevent the probe from sticking.

Automatic Test Equipment (ATE)

As manufacturers strive to increase production, the question becomes not whether to use automatic test engineering (ATE), but which ATE system to use and how much to spend on it. Because of the rapid fall in price of computers, memories, and peripherals, today's low-cost ATE equals the performance of the high-cost equipment of just two or three years ago. For factory automation, manufacturers must consider many factors, such as production volume, product complexity, and availability of skilled personnel.

One question is whether the ATE system can be used not only for production testing but also for service and repair to reduce the high cost of keeping a substrate inventory in the field. Another is whether assembly and process induced faults represent a significant percentage of production defects, rather than out-of-tolerance components. These questions need to be answered before deciding on the type of ATE system.

Several systems are currently available to the manufacturer, including short-circuit testers, in-circuit testers, in-circuit analyzers and functional testers. Figure 3 shows a bar-chart giving a comparison of percent fault detection and programming time for various ATE systems.

A loaded-board short-circuit tester takes from two to six hours to program and its effective fault coverage

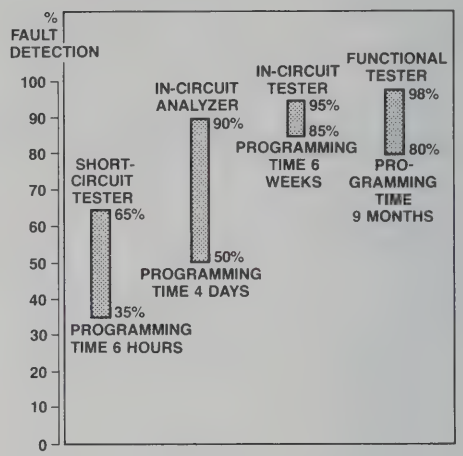


Fig. 3. Bar chart showing a comparison of percent fault detection and programming time for various ATE systems.

is between 35 and 65 percent. It has the advantage of being operationally fast and comparatively inexpensive. On the negative side, however, it is limited to the detection of short-circuits and may require a double-sided bed-of-nails test fixture (see Fig. 4), which for SMD substrates, may be expensive and take time to produce. Careful design can, however, often eliminate the need for double-sided test probe fixtures.

In-circuit testers power the assembly and check for open or short-circuits, circuit parameters, and can pin-point defective components. They can provide around 90 percent fault coverage, but are more expensive than short-circuit testers and programming can take more than six weeks.

In-circuit analyzers are relatively simple to program and can detect manufacturing-induced faults in one third of the time required by an in-circuit tester. Fault coverage is between 50 and 90 percent. Because they do not power the assembly, they cannot detect digital logic faults, unlike an in-circuit tester or functional tester.

Functional testers, on the other hand, check the assembly's performance

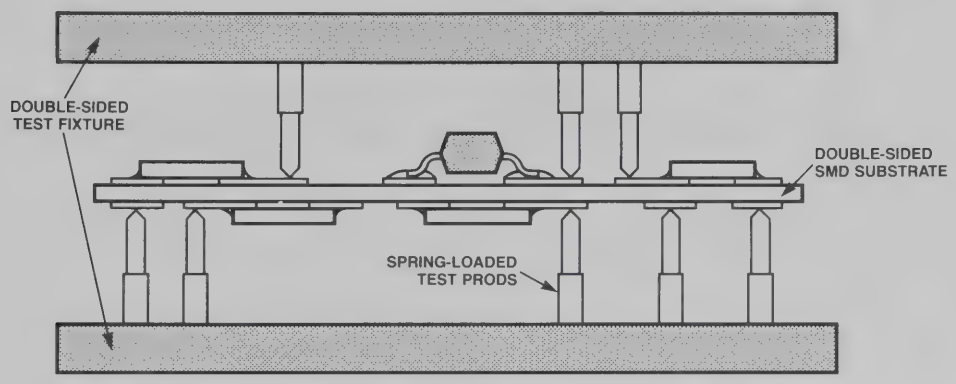


Fig. 4. Double-sided bed-of-nails test fixture.

and simply make a go or no-go decision. Either the assembly performs its required function or it does not. They are much more expensive, but their fault coverage is between 80 and 98 percent. Their major disadvantages, apart from cost, are that they cannot locate defective components, and programming for a high-capacity system can take as long as nine months.

ATE Systems

An analysis of defects on a finished substrate will determine which combination of ATE will best meet the test requirements with regard to fault coverage and throughput rate.

If most defects are short-circuits, a loaded-board short-circuit tester, in tandem with an in-circuit tester, will pre-screen the substrate for short-circuits twice as fast as the in-circuit tester. This allows more time for the in-circuit tester to handle the more complex test requirements. This combination of ATE, instead of an in-circuit tester alone, improves the throughput rate.

Combining a short-circuit tester with a functional tester, produces even more dramatic results. If most defects are manufacturing-produced shorts, the use of a short-circuit tester to relieve the functional tester of this task, can increase throughput five-fold while maintaining a fault coverage of up to 98 percent.

If manufacturing faults and analog component defects are responsible for the majority of failures, a relatively low-cost in-circuit analyzer can be used in tandem with an in-circuit tester or functional tester to reduce testing costs and improve throughput. The in-circuit analyzer is three times faster than an in-circuit tester in detecting manufacturing-induced faults, offers test and diagnostics usually within 10 seconds each, and is relatively simple to program. But because it is unpowered, an in-circuit analyzer cannot test digital logic faults; either an in-circuit tester or functional tester following the in-circuit analyzer must be used to locate this type of defect.

Polluted Power Supplies

Today's electronic components and the equipment used to test them are susceptible to electrical noise. Erroneous measurements on pass-or-fail tests could lower test throughput or, even more seriously, allow defective products to pass inspection. Semiconductor chips under test can also be damaged or destroyed as high-energy pulses or line-voltage surges stress the fine-line geometrics separating individual cells.

Noise pulses can be either in the normal (line-to-line) mode or common (line-to-ground) mode. Common-mode electrical noise poses a special threat to modern electronic circuitry since the safety ground line to which common-mode noise is referenced is often used as the system's logic reference point. Since parasitic capacitance exists between safety ground and the reference point, at high frequencies these points are essentially tied together, allowing noise to directly enter the system's logic.

Manual Repair

The repair of SMD populated substrates will entail either the resoldering of individual joints and the removal of shorts or the replacement of defective components.

The re-working of defective joints will invariably involve the use of a manual soldering iron. Bits are commercially available in a variety of shapes including special hollow bits used for desoldering and for the removal of solder bridges. The criteria for the inspection of re-worked soldered joints are the same as those for machine soldering. These are detailed in the publication titled SOLDER JOINT CRITERIA.

Special care must be taken when re-working or replacing electrostatic sensitive devices. Soldering irons should be well grounded via a safety resistor of minimum 100 k ohms. The ground connection to the soldering iron should be welded rather than clamped. This is because oxidation occurs beneath the clamp, thus isolating the ground connection. Voltage spikes caused by the switching of the iron can be avoided by using either continuously-powered irons, or irons that switch only at zero voltage on the AC sine curve.

To remove defective leadless SMDs, a variety of soldering iron bits are available that will apply the correct amount of heat to both ends of the component simultaneously and allow it to be removed from the substrate. If the substrate has been wave soldered, an adhesive will have been used, and the bond can be broken by twisting the bit. Any adhesive residue must then be removed. The same tool is then used to place and solder the new component, using either solder cream or resin-cored solder.

When a multi-leaded component, such as a plastic leaded chip carrier (PLCC) has to be removed, a heated collet can be used (see Fig. 5). The collet is positioned over the PLCC, heat is applied to the leads and solder lands automatically until the solder reflows. The collet, complete with the PLCC is then raised by vacuum. Solder cream is then re-applied to the solder lands by hand. There will be no adhesive required in this operation.

The collet is positioned over the replacement PLCC which is held in place by the slight spring pressure of the PLCC leads against the walls of the collet. The collet, complete with PLCC is then raised pneumatically and positioned over the solder lands.

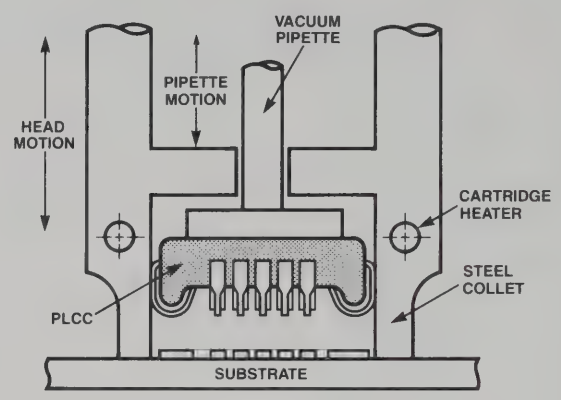


Fig. 5 Heated collet for the removal and replacement of multi-leaded SMDs (a PLCC is shown here).

Using air pressure, the center pin of the collet then pushes the PLCC into contact with the substrate where it is maintained with the correct amount of force. Heat is then applied through the walls of the collet to reflow the solder paste. The center pin maintains pressure on the PLCC until the solder has solidified, then the center pin is raised and the replacement is complete.

Another method, well suited to densely populated SMD substrates, uses a stream of heated air, directed onto the SMD terminations. Once the solder has been reflowed, the component can be removed with the aid of tweezers. While the hot air is being directed onto the component, cooler air is played onto the bottom of the substrate to protect it from heat damage. During removal, the component should be twisted sideways slightly in order to break the surface tension of the solder and any adhesive bond between the component and the substrate. This prevents damage to the substrate when the component is lifted.

To fit a new component, the solder lands are first retinned and fluxed, the new component accurately placed and the solder reflowed with hot air. Substituting superheated argon, nitrogen, or a mixture of nitrogen and hydrogen for the hot air stream removes any risk of contaminating or oxidizing the solder.

Focused infrared light has also been used successfully to reflow the solder on densely populated substrates.

In general, the equipment and procedures used for the replacement of PLCCs can be used for leadless ceramic chip carriers (LCCCs) and small-outline packages (SO ICs). SO ICs are somewhat easier to replace as the leads are more accessible and only on two sides of the component.

Packaging

SM transistors and diodes are supplied in a variety of packaging options.

Bulk product is available for prototyping and low-volume manual placement operations. Bulk devices are supplied in antistatic plastic vials with detachable lids.

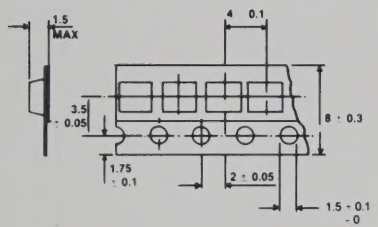
Tape & reel packaging is available to facilitate automatic placement. All SM package types are supplied in antistatic plastic cavity tape. SOD-80 MELF diodes are supplied in aluminum carrier tape. All tape & reel packaging conforms to EIA-RS481A and IEC 286-3 specifications.

Standard packaging quantities and ordering information is shown in Table 1.

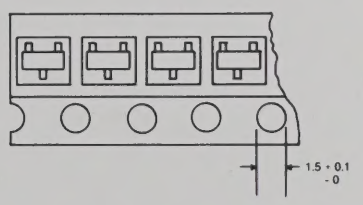
SM Package	Devices per reel	Reel Size (in)	Tape Width (mm)	Ordering Suffix
SOT-23	3K	7	8	TRL
	10K	13	8	TRL 13
SOT-89	1K	7	12	TRL
	4K	13	12	TRL 13
SOT-143	3K	7	8	TRL
	10K	13	8	TRL 13
SOD-80	2.5K	7	8	TRL
	10K	13	8	TRL 13
SOD-87	2K	7	8	TRL

Table 1

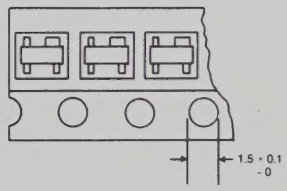
TAPE DIMENSIONS AND ORIENTATION: (Dimensions in mm)



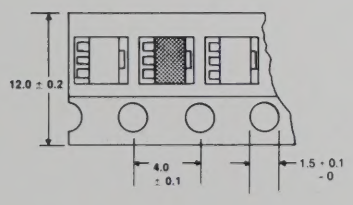
SOT-23 and SOT-143
TAPE DIMENSIONS



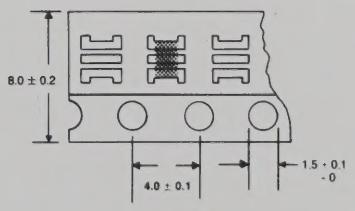
SOT-23
ORIENTATION



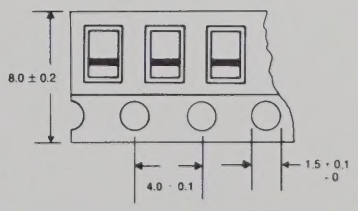
SOT-143
ORIENTATION



SOT-89
TAPE DIMENSIONS
AND ORIENTATION



SOD-80
TAPE DIMENSIONS
AND ORIENTATION
(STANDARD DIODE ORIENTATION IS
CATHODE BAND AT SPROCKET HOLE SIDE)



SOD-87
TAPE DIMENSIONS
AND ORIENTATION
(STANDARD DIODE ORIENTATION IS
CATHODE BAND AT SPROCKET HOLE SIDE)

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